10/100/1000Base-T Copper Transceiver Supporting SyncE Small Form Pluggable (SFP), 3.3V 1.25Gbps Gigabit Ethernet

Features

- Designed with Broadcom's BCM54210 chipset
- Complies with IEEE 802.3, 802.3u, and 802.3ab specifications
- Configured for operation with a SGMII compliant host
- Supports SyncE functionality (1000BASE-T connection only)
- Conforms to Multi-Source Agreement (MSA) specifications for SFP transceivers (Exceptions for SyncE features)
- Supports IEEE 802.3u and IEEE 802.3ab auto–negotiation features to allow networking equipment to automatically determine and adjust the required settings
- Supports jumbo frames up to 18 KB
- Automatic MDI crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports.
- Compact RJ45 connector assembly
- Detailed Product Information in EEPROM
- +3.3V Single Power Supply
- Access to Physical Layer IC and EEPROM via 2-wire serial bus (I2C)
- Compliant with RoHs
- Compliant with IEEE Std 802.3-2015
- Temperature range: commercial: 0°C to 70°C, industrial: -40°C to 85°C

Application

- 10/100/1000Mbps Ethernet over Category 5/5e Cable
- Networking equipment
- High speed I/O for file server or high-end workstation
- Switch/Router to Switch/Router Link

Description

The 10/100/1000Base-T SFP Copper Transceiver named as ASFPT, which supports 1000Mb/s data-rate up to 100 meters reach over twisted-pair category 5/5e cable, is high performance and built-in MCU control with Synchronous Ethernet capability for SGMII host interface. The host interface transmits and receives serial data differentially at 1.25Gbps. The copper interface is advertised as full duplex and will auto-negotiate to 10/100/1000Base-T.

In addition, the ASFPT module provides standard serial ID information compliant with SFP MSA, which can be accessed with address of A0h via the 2-wire serial CMOS EEPROM protocol. The physical IC and SyncE feature controlled by register can also be accessed via 2-wire serial bus at address ACh and A2h, respectively.

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Ordering Information

PART NUMBER	HOST INTERFACE	Rx LOS	SyncE	Auto-Negotiation	TEMPERATURE
ASFPT-T3C-I-S0	SGMII[1]	Enabled[2]	Disabled[3]	Yes	-40°C to 85°C
ASFPT-T3C-S0	SGMII	Enabled	Disabled	Yes	0°C to 70°C

Notes:
[1]SGMII is a mode of communication between MAC and PHY to allow for 10/100/1000BASE-T operation. If using GBIC mode, refer to the method of Appendix section D.
[2]RxLOS is always enabled.
[3]SyncE is defaulted as disabled. Enable SyncE functionality to refer Appendix section A, B, and E.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	-40	90	°C	Ambient
Storage Humidity	H_S	5	95	%	

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Operating Temperature (Case)	T_I	-40	-	85	°C	Industrial
Operating Temperature (Case)	T_C	0	-	70	°C	Commercial
Operating Humidity	*Ho*	10	-	85	%	
Supply Voltage	V_{CC}	3.14	3.3	3.47	V	
Supply Current	I_{CC}	-	245	-	mA	1000BASE-T

General Specifications

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Distance	C_L	-	-	100	m	Category 5/5e UTP
Line Frequency	F_{Line}		25	-	MHz	
RMS Phase Jitter	F_J	-	-	3	psRMS	1

Note:
1) 125MHz F_J = 12 kHz to 20 MHz offset frequency
25MHz F_J = 1 kHz to 5 MHz offset frequency

SyncE Specifications

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Recovered Clock Jitter		-50	±25	50	ppm	
Recovered Clock	*RCO*	-	25	-	MHz	1
Primary Reference Clock	*PRC*	-	25		MHz	±25ppm

Note:
1) 25 MHz for locally generated clock.

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Electrical Characteristics

V_{CC} = 3.3 V, T = -40 °C to +85 °C

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
SGMII Receiver						
Baud rate	R_{Baud}	-	1.25	-	Gsym/s	
Input differential threshold	$V_{I, Diff}$	250	-	1600	mVppd	1
Differential Input Impedance	Z_{IN}	-	100	-	Ω	
Disable Input-High	V_{DISH}	2.0	-	V_{cc}+0.3	V	2
Disable Input-Low	V_{DISL}	0	-	0.8	V	2
SGMII Transmitter						
Output differential voltage	$V_{O, Diff}$	600	-	1200	mVppd	1
Differential Output Impedance	Z_{OUT}	-	100	-	Ω	
Output Rise/Fall Time	T_R/T_F	100	-	200	ps	20% ~ 80%
Skew	T_{SKEW}	-20		20	ps	3
LOS Output Voltage – High	V_{SDHL}	V_{cc}-0.4	-	V_{cc}+0.3	V	2
LOS Output Voltage – Low	V_{SDL}	0	-	0.4	V	2

Note:
1) Internally AC coupled, but requires a 100Ω differential termination. R_{load} = 100Ω ± 1%.
2) Pull up to V_{CC} with a 4.7K to 10KΩ resistors on the host board.
3) Skew between two members of a differential pair.

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LOS Function

The SFP MSA specification defines a pin called LOS to indicate loss of signal to the motherboard. This should be pulled up with a 4.7K to 10K resistor. Pull up voltage between 2.0V and Vcc-T/R+0.3V. When high, this output indicates link fail. Low indicates normal operation. In the low state, the output will be pulled to <0.8V.

Termination Circuits

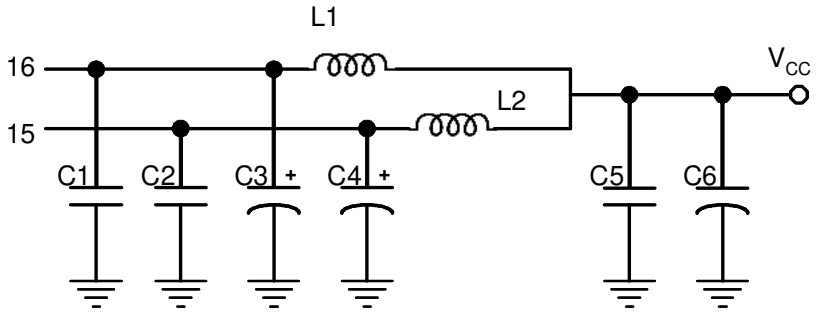
Inputs to the transceiver are AC coupled and internally terminated through 50 Ohms. These modules can operate with PECL or ECL logic levels. The input signal must have at least a 250mV peak-to-peak (single ended) signal swing. Output from the receiver section of the module is also AC coupled and is expected to drive a 50 Ohms load. Different termination strategies may be required depending on the particular Serializer/Deserializer chip set used. The transceiver is designed with AC coupled data inputs and outputs to provide the following advantages:

Close positioning of SerDes with respect to transceiver; allows for shorter line lengths and at Gigabit speeds reduces EMI. It has minimum number of external components. Internal termination reduces the potential for un-terminated stubs which would otherwise increase jitter and reduce transmission margin.

Subsequently, this affords the customer the ability to optimally locate the SerDes as close to the transceiver as possible and save valuable real estate. At Gigabit rates this can provide a significant advantage resulting in better transmission performance and accordingly better signal integrity.

Power Coupling

A suggested layout for power and ground connections is given in Figure 1 below. Connections are made via separate voltage and ground planes. The mounting posts are at case ground and should not be connected to circuit ground. The ferrite bead should provide a real impedance of 50 to 100 Ohms at 100 to 1000 MHz. Bypass capacitors should be placed as close to the 20 pin connector as possible.



VALUES:
C1, C2, C5 = 0.1µF
C3, C4, C6 = 10 µF, Tantalum
L1, L2 = 1 µH

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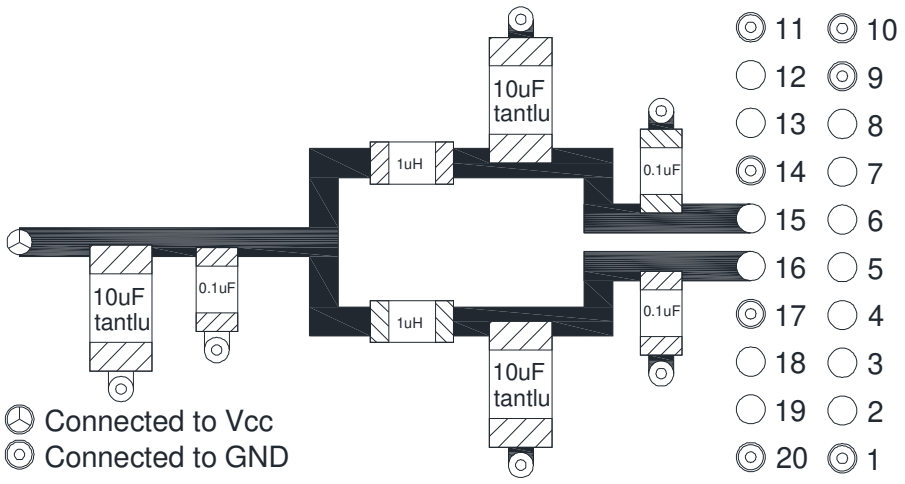

Figure 1: Suggested Power Coupling

Serial Communication Protocol

The ASFPT module supports the 2-wire serial communication protocol defined in the SFP MSA and uses a 256-byte EEPROM with an address of A0h to store Table 1 data. The PHY IC and SyncE control register can also be accessed directly via the 2-wire serial bus at address ACh and A2h, respectively.

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EEPROM Serial ID Memory Contents

Accessing Serial ID Memory uses the 2 wire address 10100000 (A0h). Memory Contents of Serial ID are shown in Table 1.

Table 1 Serial ID Memory Contents

Addr.	Size (Bytes)	Name of Field	Hex	Description
0	1	identifier	03	SFP or SFP+
1	1	Ext.Identifier	04	GBIC/SFP function is defined by two-wire interface ID only
2	1	Connector	22	RJ45
3-10	8	Transceiver	00 00 00 08 00 00 00 00	Transceiver Code
11	1	Encoding	01	8B/10B
12	1	BR(Nominal)	0D	1300Mbps
13	1	Rate Identifier	00	Unspecified
14	1	Length(SMFm)-km	00	N/A
15	1	Length(SMF)	00	N/A
16	1	Length(50μm)	00	N/A
17	1	Length(62.5μm)	00	N/A
18	1	Length(cable)	64	100(units of meters)
19	1	Length(OM3)	00	N/A
20-35	16	Vendor name	XX XX XX XX XX XX XX 20 20 20 20 20 20 20 20 20	Vendor name (ASCII)
36	1	Transceiver	00	Unallocated
37-39	3	Vendor OUI	XX XX XX	Vendor OUI
40-55	16	Vendor PN	XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX	Transceiver part number
56-59	4	Vendor rev	XX XX XX XX	Vendor rev
60-61	2	Wavelength	00	0nm
62	1	Unallocated	00	Unallocated
63	1	CC_BASE	Check Sum (Variable)	Check code for Base ID Fields
64-65	2	Options	00 12	TX_Disable and LOS implemented
66	1	BR	00	max
67	1	BR	00	min
68-83	16	Vendor SN	41 34 32 30 33 30 30 34 20 20 20 20 20 20 20 20	Serial Number of transceiver (ASCII). For example“A4203004”.
84-91	8	Date code	XX XX XX XX XX XX XX XX	Manufacture date code
92	1	Diagnostic Monitoring Type	00	N/A
93	1	Enhanced Options	00	N/A
94	1	SFF-8472 Compliance	00	Digital diagnostic function not included or undefined
95	1	CC_EXT	Check Sum (Variable)	Check sum for Extended ID Field.
96-127	32	Vendor Specific	Read only	Depends on customer information

Note: The “XX” byte should be filled in according to practical case. For more information, please refer to the related document of SFP Multi-Source Agreement (MSA).

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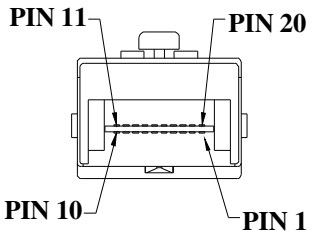
Connection Diagram

Pin-Out



Pin	Signal Name	Function	Descript	Notes
1	VeeT	Transmitter Ground	VeeT and VeeR are connected in SFP.	7
2	TX_FAULT	Transmitter Fault Indication	Not supported and Clock Output is disabled. *(default)*	1
	RCO	Synchronous Ethernet Clock	125MHz clock locally generated	8
			Recovered Clock	8, 9, 10
3	TX_DISABLE	Transmitter Disable	Module disables on high or open	2
4	MOD DEF (2)	Module Definition 2	Data Line (SDA) for Serial ID.	3
5	MOD DEF (1)	Module Definition 1	Clock Line (SCL) for Serial ID.	3
6	MOD DEF (0)	Module Definition 0	Grounded within the module	3
7	RATE SELECT	Not Implemented	No connection required. *(default)*	
	PRC	Primary reference clock	25MHz frequency input	8, 10
8	LOS	Loss of Signal	See LOS option. *(default)*	
	PHY_INT	PHY Interrupt	Logic ‘0’ when PHY interrupt occurred, ‘1’ otherwise	10
9	VeeR	Receiver Ground	VeeT and VeeR are connected in SFP.	7
10	VeeR	Receiver Ground	VeeT and VeeR are connected in SFP.	7
11	VeeR	Receiver Ground	VeeT and VeeR are connected in SFP.	7
12	RD-	Inverted Received Data out	AC coupled 100 ohm differential high speed data lines.	4
13	RD+	Non-Inverted Received Data out	AC coupled 100 ohm differential high speed data lines.	4
14	VeeR	Receiver Ground	VeeT and VeeR are connected in SFP.	7
15	VccR	Receiver Power	VccR and VccT are connected in SFP.	5
16	VccT	Transmitter Power	VccR and VccT are connected in SFP.	5
17	VeeT	Transmitter Ground	VeeT and VeeR are connected in SFP.	7
18	TD+	Non-inverted Data In	AC coupled 100 ohm differential high speed data lines.	6
19	TD-	Inverted Data In	AC coupled 100 ohm differential high speed data lines	6
20	VeeT	Transmitter Ground	Veet and VeeR are connected in SFP	7

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Notes:

1. TX Fault is not used and is always tied to ground.
2. TX disable is an input that is used to reset the chip of Gigabit Ethernet PHY inside the copper SFP. It is pulled up within the module with a 4.7-10 K Ohms resistor. Disable (PHY IC Disabled) >2V or open, Enable (PHY IC on) < 0.8V.
3. Mod-Def 0, 1, 2 are the module definition pins. They should be pulled up with a 4.7-10K Ohms resistor on the host board to a supply between 2V and 3.6V.
4. RD-/+: These are the differential receiver outputs. They are ac coupled 100 Ohms differential lines which should be terminated with 100 ohm differential at the user SerDes. The ac coupling is done inside the module and is thus not required on the host board. The voltage swing levels are compatible with CML and LVPECL voltage swings.
5. VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.3 V ± 5% at the SFP connector pin.
6. TD-/+: These are the differential transmitter inputs. They are ac coupled differential lines with 100 Ohms differential termination inside the module. The ac coupling is done inside the module and is thus not required on the host board. The inputs levels are compatible with CML and LVPECL voltage swings.
7. Circuit ground is connected to chassis ground.
8. Clock output is enabled by set RCO Control flag in “SyncE Control” and recovered clock is enabled by “Recovered Clock Control”.
9. Recovery Clock:
   - Link-down: 25 Mhz clock locally generated
   - 1000BASE-T: 25Mhz clock recovered from line-side data
   - 100BASE-TX: 25Mhz clock recovered from line-side data
   - 10BASE-T: 2.5Mhz clock recovered from line-side data
10. PHY configuration also required.

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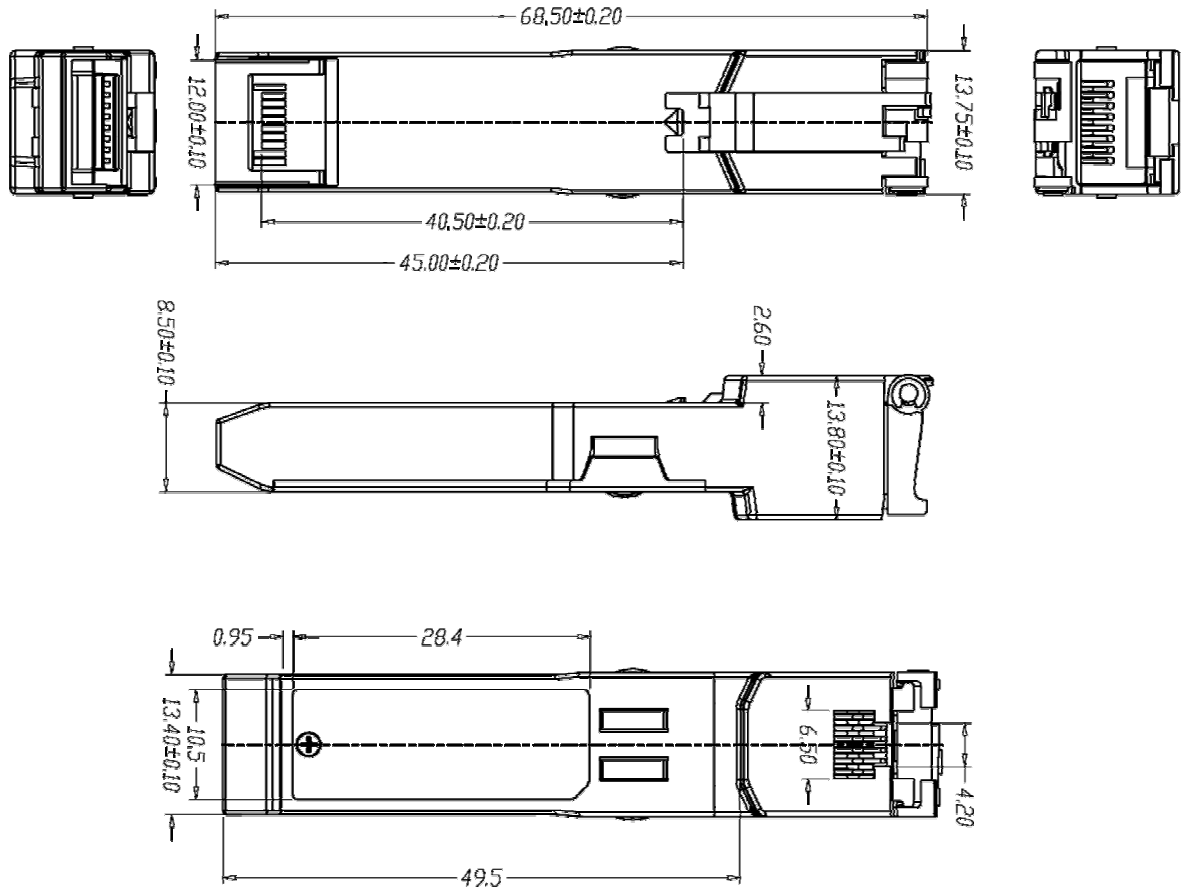
Drawing Dimensions



UNIT: mm

Mating of SFP Transceiver to SFP Host Board Connector

The pads on the PCB of the SFP transceiver shall be designed for a sequenced mating as follows: First mate: Ground contacts. Second mate: Power contacts. Third mate: Signal contacts The SFP MSA specification for a typical contact pad plating for the PCB is 0.38 micrometers minimum hard gold over 1.27 micrometers minimum thick nickel. To ensure the long term reliability performance after a minimum of 50 insertion removal cycles, the contact plating of the transceiver is 0.762 micron (30 micro-inches) over 3.81 micron (150 micro-inches) of Ni on Cu contact pads.

RJ45 Connector

RJ45 connector shall support shielded and unshielded cables. Also, the connector is mechanically robust enough and designed to prevent loss of link, when the cable is positioned or moves in different angles. The connector shall pass the "wiggle" RJ45 connector operational stress test. During the test, after the cable is plugged in, the cable is moved in circle to cover all 360 deg in the vertical plane, while the data traffic is on. There shall be no link or data loss.

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Appendix:

A. SyncE Control Register (Default 0xBF)

Bit	Name	Description	Default Value
7	Reserved	Write 1 only	1
6	Host Interface	1 = GBIC 0 = SGMII	0
5	Low Power Mode	1 = Low power mode released 0 = Low power mode active	1
4	PHY Reset Line	1 = PHY Reset line released 0 = PHY Reset line active	1
3	RCO Mode	1 = Normal RCO (2.5/25/125MHz) 0 = Restrict clock to 25MHz	1
2	RCO Control	1 = disable Clock Output (pin 2) 0 = enable Clock Output (pin 2)	1
1	LOS / PHY Interrupt	1 = LOS functionality (pin 8) 0 = PHY Interrupt indication (pin 8)	1
0	Clock Source Select	1 = internal 25MHz Oscillator 0 = external Primary Reference Clock (pin 7) Input	1

Note: *direct access by write/read configuration byte to/from I2C device with any register address under A2h address.*

B. Recovered Clock Control

I2C Address	Control Register	Byte 1	Byte 2	Description
AC	17	0F	44	Disable Recovered Clock (default)
AC	15	00	00	
AC	17	0F	44	Enable Recovered Clock
AC	15	00	10	

Note: *in HEX value*

C. Advertise 1000BASE-T full duplex capability and Master / Slave Configuration

I2C Address	Control Register	Byte 1	Byte 2	Description
AC	09	02	00	Automatic Master/Slave configuration (default)
AC	09	1A	00	Configure SFP as Master
AC	09	12	00	Configure SFP as Slave

Note: *in HEX value*

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D. Interface Selection

At power up, the ASFPT module can be configured in GBIC or SGMII mode. The user may select a different host interface using one of the following methods:

1) Method 1

I2C Address	Control Register	Byte 1	Byte 2	Description
AC	1C	FC	FE	Set mode to GBIC*
AC	1C	FC	FC	Set mode to SGMII (default)

Note: *in HEX value*
**please also clear related Auto-Negotiation Advertisement bits in PHY Register 04h.*

2) Method 2

I2C Address	Configure Byte	Description
A2	EF	Set mode to GBIC mode PHY Reset line active
-	-	Wait, at least 10 ms
A2	FF	Release PHY Reset line
-	-	Wait, at least 20 μs

Note: *in HEX value*

E. List of Supported IEEE Defined PHY Registers

Register	Name
00h	Control
01h	Status
02h-03h	PHY Identification
04h	Auto-Negotiation Advertisement
05h	Auto-Negotiation Link Partner Ability
06h	Auto-Negotiation Expansion
07h	Next Page Transmit
08h	Link Partner Received Next Page
09h	1000Base-T Control
0Ah	1000Base-T Status
0Fh	Extended Status
19h	Auxiliary Status Register

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1) PHY Register 00h: Control

Bit	Name	Description	R/W	Default
15	Reset	Software Reset 1 = PHY reset 0 = normal operation	R/W *Self-Clearing	0
14	Loopback	Internal loopback mode 1 = enable loopback mode 0 = disable loopback mode	R/W	0
13	Speed Selection (LSB)	When auto-negotiation is disabled, bits 6 and 13 can be used to manually select the speed of operation Bits [6, 13] 11 = Reserved 10 = 1000Mbps 01 = 100Mbps 00 = 10Mbps	R/W	0
12	Auto-Negotiation Enable	If enabled, Auto-Negotiation result overrides Speed Selection, Duplex Mode settings. 1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W	1
11	Power Down	Placed SFP in a low-power mode. 1 = power down 0 = normal operation	R/W	0
10	Isolate	1 = isolate 0 = normal operation	R/W	0
9	Restart Auto-Negotiation	When auto-negotiation is enabled, setting this bit restarts the Auto-Negotiation process. 1 = restart Auto-Negotiation process 0 = normal operation	R/W *Self-Clearing	0
8	Duplex Mode	1 = full duplex 0 = half duplex	R/W	1
7	Reserved	Write as 0, ignore on read	R/W	0
6	Speed Selection (MSB)	Use in conjunction with bit 13	R/W	1
5:0	Reserved	Write as zero, ignore on read	R/W	0x00

2) PHY Register 01h: Status (default 0x7949)

Bit	Name	Description	R/W	Default
15	100BASE-T4	100BASE-T4 protocol is not supported. 0 = not capable to perform 100BASE-T4	RO	0
14	100BASE-TX Full Duplex	1 = capable to perform full duplex 100BASE-TX 0 = not capable to perform full duplex 100BASE-TX	RO	1
13	100BASE-TX Half Duplex	1 = capable to perform half duplex 100BASE-TX 0 = not capable to perform half duplex 100BASE-TX	RO	1
12	10Base-T Full Duplex	1 = capable to operate at 10Base-T in full duplex mode 0 = not capable to operate at 10Base-T in full duplex mode	RO	1
11	10Base-T Half Duplex	1 = capable to operate at 10Base-T in half duplex mode 0 = not capable to operate at 10Base-T in half duplex mode	RO	1
10	100BASE-T2 Full Duplex	100BASE-T2 protocol is not supported. 0 = not capable to perform full duplex 100BASE-T2	RO	0
9	100BASE-T2 Half Duplex	100BASE-T2 protocol is not supported. 0 = not capable to perform half duplex 100BASE-T2	RO	0
8	Extended Status	1 = extended status information in register 0x0Fh 0 = no extended status information in register 0x0Fh	RO	1

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7	Reserved	Ignore on read	RO	0
6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not	RO	1
5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO	0
4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO	0
3	Auto-Negotiation Ability	1 = capable to perform Auto-Negotiation	RO	1
2	Link Status	1 = link is up 0 = link is down	RO	0
1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO	0
0	Extended Capability	1 = extended register capabilities 0 = basic register set capabilities only	RO	1

3) PHY Register 02h-03h: PHY Identifier

Bit	Name	Description	R/W	Default
15:0	Address 02h: PHY ID (MSB)	MSB of PHY Identifier	RO	0x600D
15:10	Address 03h: PHY ID (LSB) – OUI	LSB of PHY Identifier (* - PHY Rev Number)	RO	0x859n
9:4	Address 03h: Model	Device model number		
3:0	Address 03h: Revision	Device revision number		

Note that the n is the revision number. In the B0 version of the BCM54210, the read value of register 03h is 8599h.

4) PHY Register 04h: Auto-Negotiation Advertisement (default 0x01E1)

Bit	Name	Description	R/W	Default
15	Next Page	1 = Next Page capable 0 = no Next Page capability	R/W	0
14	Reserved	Write as zero, ignore on read	R/W	0
13	Remote Fault	1 = remote fault supported 0 = no remote fault	R/W	0
12	Reserved	Write as zero, ignore on read	R/W	0
11	Asymmetric Pause	1 = advertise asymmetric pause 0 = advertise no asymmetric pause	R/W	0
10	Pause Capable	1 = capable of full duplex pause operation 0 = not capable of pause operation	R/W	0
9	100BASE-T4 Capable	100BASE-T4 protocol is not supported. Do not write 1. 0 = not capable to perform 100BASE-T4	R/W	0
8	100BASE TX Full Duplex Capable	1 = 100BASE-TX full duplex capable 0 = Not 100BASE-TX full duplex capable	R/W	1
7	100BASE-TX Half Duplex Capable	1 = 100BASE-TX half duplex capable 0 = Not 100BASE-TX half duplex capable	R/W	1
6	10BASE-T Full Duplex Capable	1 = 10BASE-T full duplex capable 0 = Not 10BASE-T full duplex capable	R/W	1
5	10BASE-T Half Duplex Capable	1 = 10BASE-T half duplex capable 0 = Not 10BASE-T half duplex capable	R/W	1
4:0	Protocol Selector Field	Selector Field mode: 00001 = IEEE 802.3 CSMA/CD.	R/W	0x01

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5) PHY Register 05h: Auto-Negotiation Link Partner Ability (default 0x0000)

Bit	Name	Description	R/W	Default
15	Next Page	1 = link partner capable of Next Page 0 = link partner not capable of Next Page	RO	0
14	Acknowledge	1 = link partner has received link code word 0 = link partner has not received link code word	RO	0
13	Remote Fault	1 = link partner has detected remote fault 0 = link partner has not detected remote fault	RO	0
12	Reserved	Write as zero, ignore on read	RO	0
11	Asymmetric Pause	1 = link partner wants asymmetric pause 0 = link partner does not want asymmetric pause	RO	0
10	100BASE-T4 Capable	1 = link partner is capable of pause operation 0 = link partner is not capable of pause operation	RO	0
9	100BASE-T4 Capable	1 = link partner is 100BASE-T4 capable 0 = link partner is not 100BASE-T4 capable	RO	0
8	100BASE-TX Full Duplex Capable	1 = link partner is 100BASE-TX full duplex capable 0 = link partner is not 100BASE-TX full duplex capable	RO	0
7	100BASE-TX Half Duplex Capable	1 = link partner is 100BASE-TX half duplex capable 0 = link partner is not 100BASE-TX half duplex capable	RO	0
6	10BASE-T Full Duplex Capable	1 = Link partner is 10BASE-T full duplex capable 0 = Link partner is not 10BASE-T full duplex capable	RO	0
5	10BASE-T Half Duplex Capable	1 = link partner is 10BASE-T half duplex capable 0 = link partner is not 10BASE-T half duplex capable	RO	0
4:0	Protocol Selector Field	Link partner protocol selector field	RO	0x00

6) PHY Register 06h: Auto-Negotiation Expansion (default 0x0064)

Bit	Name	Description	R/W	Default
15:7	Reserved	Write as zero, ignore on read	RO	0x00
6	Receive Next Page Location Able	1 = bit 5 determines Next Page receive location. 0 = bit 5 does not determine Next Page receive location	RO	1
5	Received Next Page Storage Location	1 = link partner Next Pages are stored in Register 8 0 = link partner Next Pages are stored in Register 5	RO	1
4	Parallel Detection Fault	1 = a fault has been detected via the Parallel Detection function 0 = a fault has not been detected via the Parallel Detection function	RO	0
3	Link Partner Next Page Able	1 = link Partner is Next Page able 0 = link Partner is not Next Page able	RO	0
2	Next Page Able	1 = local Device is Next Page able 0 = local Device is not Next Page able	RO	1
1	Page Received	1 = a New Page has been received 0 = a New Page has not been received	RO	0
0	Link Partner Auto-Negotiation Able	1 = link Partner is Auto-Negotiation able 0 = link Partner is not Auto-Negotiation able	RO	0

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7) PHY Register 07h: Next Page Transmit (default 0x2001)

Bit	Name	Description	R/W	Default
15	Next Page	1 = additional Next Pages to follow 0 = last Next Page	R/W	0
14	Reserved	Write as zero, ignore on read	RO	0
13	Message Page	1 = message page 0 = unformatted page	R/W	1
12	Acknowledge 2	1 = complies with message 0 = cannot comply with message	R/W	0
11	Toggle1	Toggles between exchanges of different Next Pages	RO	0
10:0	Message/Unformatted Code field	Next Page message code or unformatted data	R/W	0x001

8) PHY Register 08h: Link Partner Received Next Page (default 0x0000)

Bit	Name	Description	R/W	Default
15	Next Page	1 = additional Next Pages to follow 0 = last Next Page	RO	0
14	Acknowledge	1 = acknowledge 0 = no acknowledge	RO	0
13	Message Page	1 = message page 0 = unformatted page	RO	0
12	Acknowledge 2	1 = complies with message 0 = cannot comply with message	RO	0
11	Toggle2	Toggles between exchanges of different Next Pages	RO	0
10:0	Message Code field	Next Page message code or unformatted data	RO	0x000

9) PHY Register 09h: 1000Base-T Control (default 0x0200)

Bit	Name	Description	R/W	Default
15:13	Test mode bits	000 = normal operation 001 = test mode 1—Transmit waveform test 010 = test mode 2—Master transmit jitter test 011 = test mode 3—Slave transmit jitter test 100 = test mode 4—Transmitter distortion test 101, 110, 111 = reserved	R/W	0x0
12	Master/Slave Manual Config Enable	1 = manual Master/Slave configuration 0 = automatic Master/Slave configuration	R/W	0
11	Master/Slave Config Value	1 = configure PHY as Master 0 = configure PHY as Slave This bit is ignored if bit 12 = 0.	R/W	0
10	Port type	1 = indicate the preference to operate as multiport device 0 = indicate the preference to operate as single-port device	R/W	0
9	1000BASE-T Full Duplex	1 = advertise 1000BASE-T full duplex capability 0 = advertise no 1000BASE-T full duplex capability	R/W	1
8	1000BASE-T Half Duplex	1 = advertise 1000BASE-T half duplex capability 0 = advertise no 1000BASE-T half duplex capability	R/W	0
7:0	Reserved	Write as 0, ignore on read	R/W	0x00

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10) PHY Register 0Ah: 1000Base-T Status (default 0x0000)

Bit	Name	Description	R/W	Default
15	Master/Slave configuration fault	1 = Master/Slave configuration fault detected 0 = No Master/Slave configuration fault detected	RO	0
14	Master/Slave configuration resolution	1 = Local transmitter is Master 0 = Local transmitter is Slave	RO	0
13	Local Receiver Status	1 = Local receiver OK 0 = Local receiver not OK	RO	0
12	Remote Receiver Status	1 = Remote Receiver OK 0 = Remote Receiver not OK	RO	0
11	LP 1000T FD	1 = Link partner is capable of 1000BASE-T full duplex 0 = Link partner is not capable of 1000BASE-T full duplex	RO	0
10	LP 1000T HD	1 = Link partner is capable of 1000BASE-T half duplex 0 = Link partner is not capable of 1000BASE-T half duplex	RO	0
9:8	Reserved	Write as zero, ignore on read	RO	0x0
7:0	Idle Error Count	Indicate the idle Error count, since last read	RO	0x00

11) PHY Register 0Fh: Extended Status (default 0x3000)

Bit	Name	Description	R/W	Default
15	1000BASE-X Full Duplex	1 = 1000BASE-X full duplex capable 0 = Not 1000BASE-X full duplex capable	RO	0
14	1000BASE-X Half Duplex	1 = 1000BASE-X half duplex capable 0 = Not 1000BASE-X half duplex capable	RO	0
13	1000BASE-T Full Duplex	1 = 1000BASE-T full duplex capable 0 = Not 1000BASE-T full duplex capable	RO	1
12	1000BASE-T Half Duplex	1 = 1000BASE-T half duplex capable 0 = Not 1000BASE-T half duplex capable	RO	1
11:0	Reserved	Write as zero, ignore on read	RO	0x000

12) PHY Register 19h: Auxiliary Status Register (default 0x0000)

Bit	Name	Description	R/W	Default
15	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO	0
14:11	Reserved	Reserved.	RO	0x0
10:8	Current Operating Speed and Duplex mode	000 = Link has not been established 001 = 10BASE-T half-duplex 010 = 10BASE-T full-duplex 011 = 100BASE-TX half-duplex 100 = 100BASE-T4 101 = 100BASE-TX full-duplex 110 = 1000BASE-T half-duplex 111 = 1000BASE-T full-duplex	RO	0x0
7	Parallel Detection Fault	1 = Parallel link fault detected 0 = Parallel link fault not detected	RO	0
6	Remote Fault	1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault	RO	0
5	Page Received	1 = New page has been received from link partner 0 = New page has not been received	RO	0

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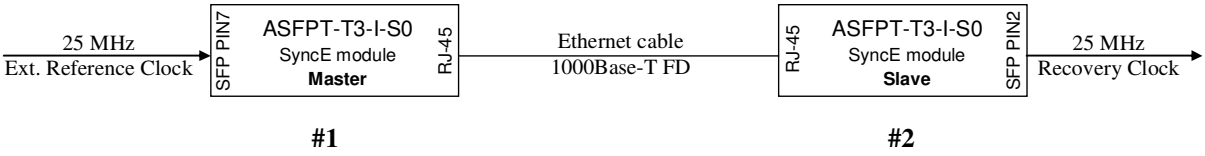
4	Link Partner Auto-Negotiation Ability	1 = Link partner has Auto-Negotiation capability 0 = Link partner does not perform Auto-Negotiation	RO	0
3	Link Partner Next Page Ability	1 = Link partner has next Page capability 0 = Link partner does not have Next Page capability	RO	0
2	Link Status	1 = Link status is OK 0 = Link status is not OK	RO	0
1	Pause Resolution RX	1 = Enable pause receive 0 = Disable pause receive	RO	0
0	Pause Resolution TX	1 = Enable pause transmit 0 = Disable pause transmit	RO	0

F. SyncE Configuration Example

The recovered clock is 25MHz when the ASFPT module is linked in 1000BASE-T Slave modes. In 1000BASE-T mode, to output the recovery clock from the link partner, the ASFPT module must auto-negotiate to Slave mode. If the ASFPT module auto-negotiates to master mode, the ASFPT module would recover its own clock, not the clock of the link partner. 10BASE-T is Manchester encoder, and the clock phase information is only transmitted when a packet is being transmitted, so 10BASE-T cannot be used for Synchronous Ethernet.



#1 Enabled primary reference 25MHz clock input on pin 7 for the SFP in Master mode - SyncE Configuration Sequence

I2C Address	Control Register/ Config. Byte	Byte 1	Byte 2	Description
A2	FE	-	-	Enable external Primary Reference Clock Input (pin 7)
AC	09	1A	00	Configure SFP as manual Master mode (1000BASE-T full duplex)
AC	00	13	40	Restart Auto-Negotiation

Note: *in Hex value*

#2 Enabled recovery clock output on pin 2 for the SFP in Slave mode - SyncE Configuration Sequence

I2C Address	Control Register/ Config. Byte	Byte 1	Byte 2	Description
AC	17	0F	44	Enable Clock Data Recovery Process
AC	15	00	10	
A2	BB	-	-	Enable Clock Output (pin 2)
AC	09	12	00	Configure SFP as manual Slave mode (1000BASE-T full duplex)
AC	00	13	40	Restart Auto-Negotiation

Note: *in Hex value*

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