



QSFP+ 40GBASE-LR4 Transceiver

Compliance with the 40GBASE-LR4 of the IEEE 802.3ba standard.
1310nm CWDM for up to 10km reach



Description

APAC QSFP+ 40GBASE-LR4 transceiver is a new high speed module with a LC connector. This interconnecting module offers 4 channels and maximum bandwidth of 40Gbps. The module consist 4x10Gbps CWDM LDs and multiplex 4 CWDM signals on a 40Gbps optical transmission, and de-multiplex 40G receiver signals to 4 CWDM signals.

Features

- Compliant with 40G Ethernet IEEE 802.3ba
- Power dissipation < 3.5W
- Full Digital Diagnostics Monitor Interface
- Up to 10km transmission on SMF
- RoHS-6 Compliant (lead-free)
- Class 1 Laser Product complies with IEC/EN60825-1: 2007 and IEC/EN60825-1: 2014

Application

- 40G Ethernet
- OTN OTU3
- Data Center Interconnects

Ordering information

PART NUMBER	DISTANCE	TEMPERATURE	NOTE
LB3C-K3S-TC-N-TF	10 km	0°C to 70 °C	4X10Gbps CWDM
LB3C-K3S-TI-N-TF	10 km	-40°C to 85 °C	4X10Gbps CWDM

Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T _s	-40	85	°C	
Power Supply Voltage	V _{cc}	-0.5	3.6	V	
Relative Humidity	RH	5	85	%	

Recommend Operating Condition



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PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Case Temperature	Tc	-40		85	°C	0~70°C for TC
Power Supply Voltage	Vcc	3.14	3.3	3.47	V	
Power Dissipation				3.5	W	

Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	-40 to 85	± 5	°C	Internal
Voltage	3.0 to 3.6	± 0.1	V	
Bias Current	5 to 70	± 10%	mA	
TX Power	-7 to +2.3	± 3 dB	dBm	
RX Power	-14.4 to 2.5	± 3 dB	dBm	

Transmitter Optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Total Average Launch Power	Pt			8.3	dBm	
Extinction Ratio	ER	3.5			dB	
Center Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
	Output Power: Average	Po	-7		2.3	dBm
Optical Modulation Amplitude, per lane	OMA	-4		3.5	dBm	
Side Mode Suppression	SMSR	30			dB	
Relative Intensity Noise	RIN20OMA			-128	dB/Hz	
Transmitter Reflectance	RT			-12	dB	
Transmitter and Dispersion Penalty	TDP			2.3	dB	
Differential Input Voltage	V _{DIFF}	0.19	---	0.7	V	
Disable Output Power	Po_off			-30	dBm	

Output Eye Mask Compliant with IEEE 802.3ba

Note1. Minimum value is informative.

Receiver Optical characteristics



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PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Damage Threshold, per lane	Pth	3.3			dBm	
Average power at receiver input, per lane		-13.7		2.3	dBm	
Receiver Power (OMA), per lane				3.5	dBm	
Receiver Sensitivity (OMA), per lane	Rsens			-11.5	dBm	
Stressed Receiver Sensitivity, per lane				-9.6	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-15	dBm	
Hysteresis	Hys	0.5		6	dB	
Receiver reflectance	RR			-26.0	dB	

Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate, per lane			10.3125		Gbps	
LP Mode/Reset/ModselL	VIL	0		0.8	V	
LP Mode/Reset/ModselL	VIH	2		Vcc+0.3	V	
ModPrsL/IntL	VOL	0		0.4	V	
ModPrsL/IntL	VOH	2		Vcc+0.3	V	

Timing for soft control/ status function / squelch & disable

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Initialization time	T_init			2000	ms	
Reset Init Assert time	T_reset_init			2	us	
Serial Bus Hardware Ready Time	T_serial			2000	ms	
Monitor Data Ready Time	T_data			2000	ms	
Reset Assert Time	T_seset			2000	ms	
LP Mode Assert time	Ton_LPMode			100	us	
LP Mode Deassert time	Toff_LPMode			300	ms	
IntL Assert Time	Ton_IntL			200	ms	
IntL Deassert Time	Toff_IntL			500	us	
Rx LOS Assert Time	Ton_los			100	ms	



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Tx Fault Assert time	Ton_Txfault	200	ms
Flag Assert Time	Ton_flag	200	ms
Tx Squelch Assert Time	Ton_Txsq	400	ms
Tx Squelch Deassert Time	Toff_Txsq	400	ms
Tx Disable Assert Time	Ton_Txdis	100	ms
Tx Disable Deassert Time	Toff_Txdis	400	ms

Pad assignment and Description

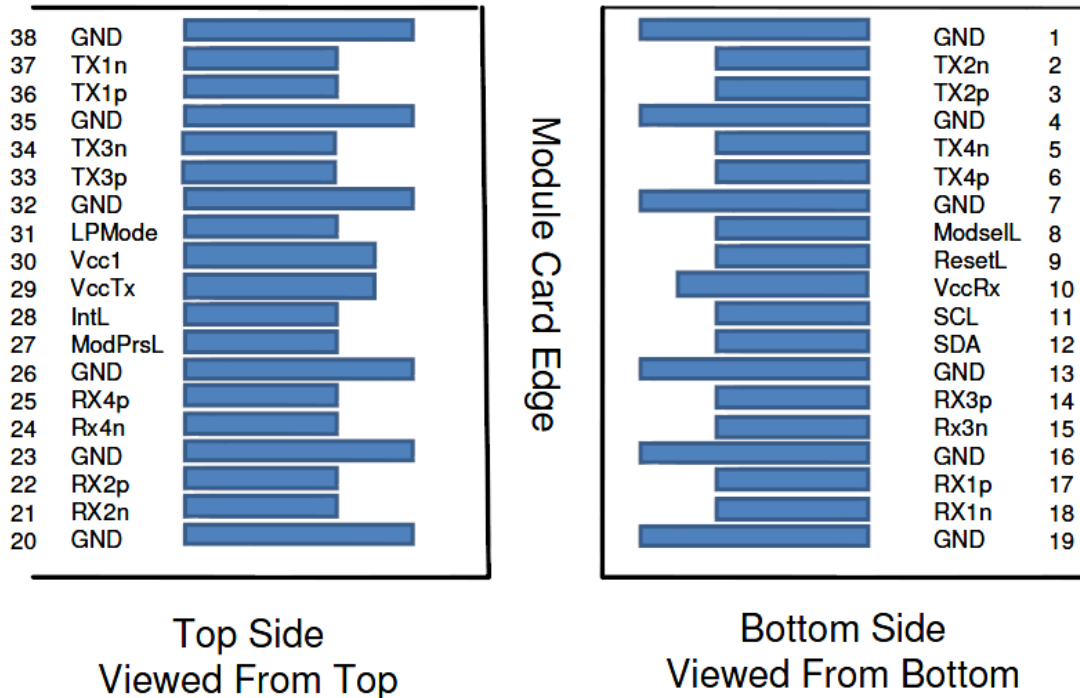
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"PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
1		GND	Ground	1	Note 1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	Note 1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	Note 1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	Note 2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	Note 2
14	CML-O	Rx3p	Receiver Non- Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	Note 1
17	CML-O	Rx1p	Receiver Non- Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	Note 1
20		GND	Ground	1	Note 1



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21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2P	Receiver Non- Inverted Data Output	3	
23		GND	Ground	1	Note 1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non- Inverted Data Output	3	
26		GND	Ground	1	Note 1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29	LVC MOS-I/O	Vcc Tx	+3.3V Power Supply transmitter	2	Note 2
30		Vcc1	+3.3V Power Supply	2	Note 2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	Note 1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	Note 1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	Note 1

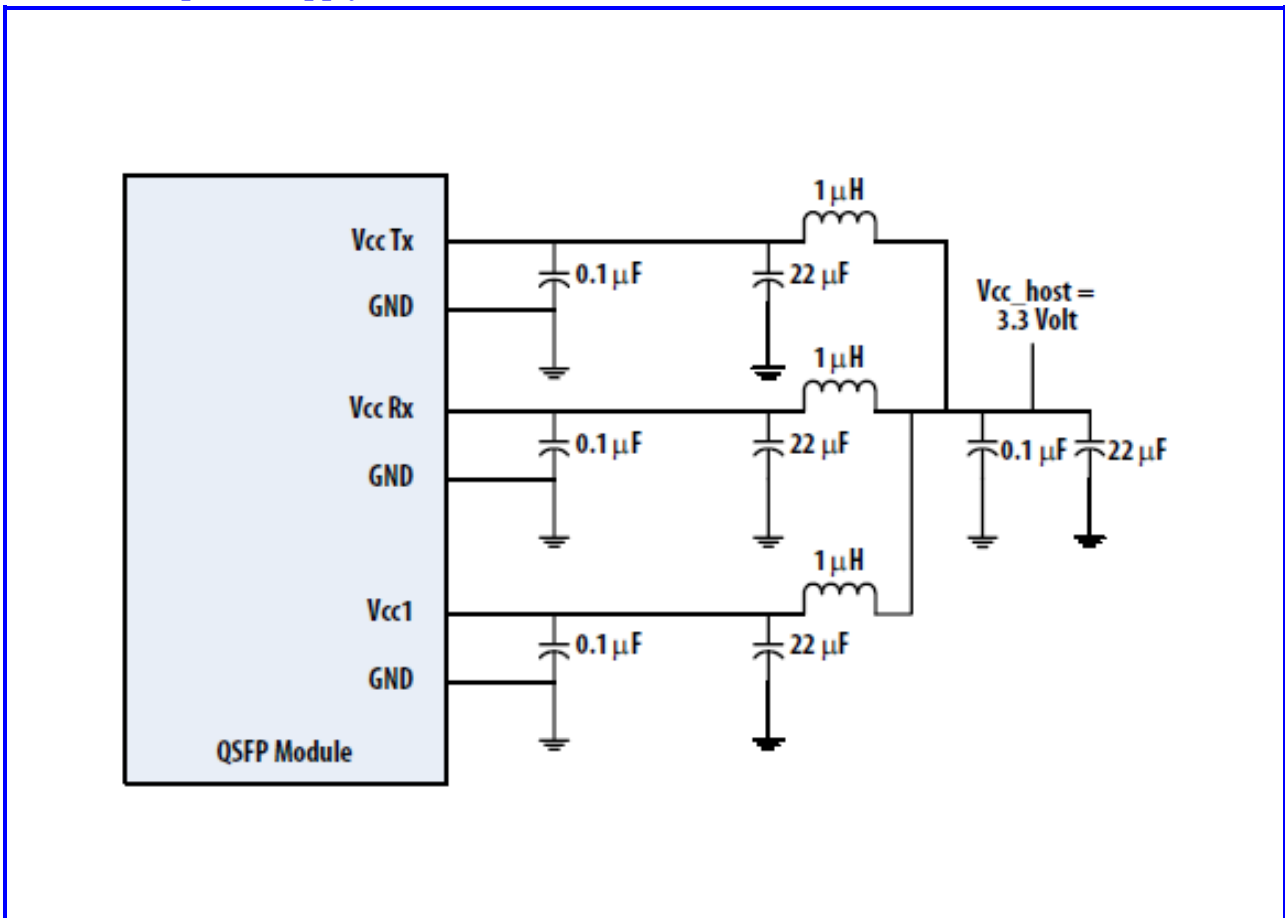
Note 1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

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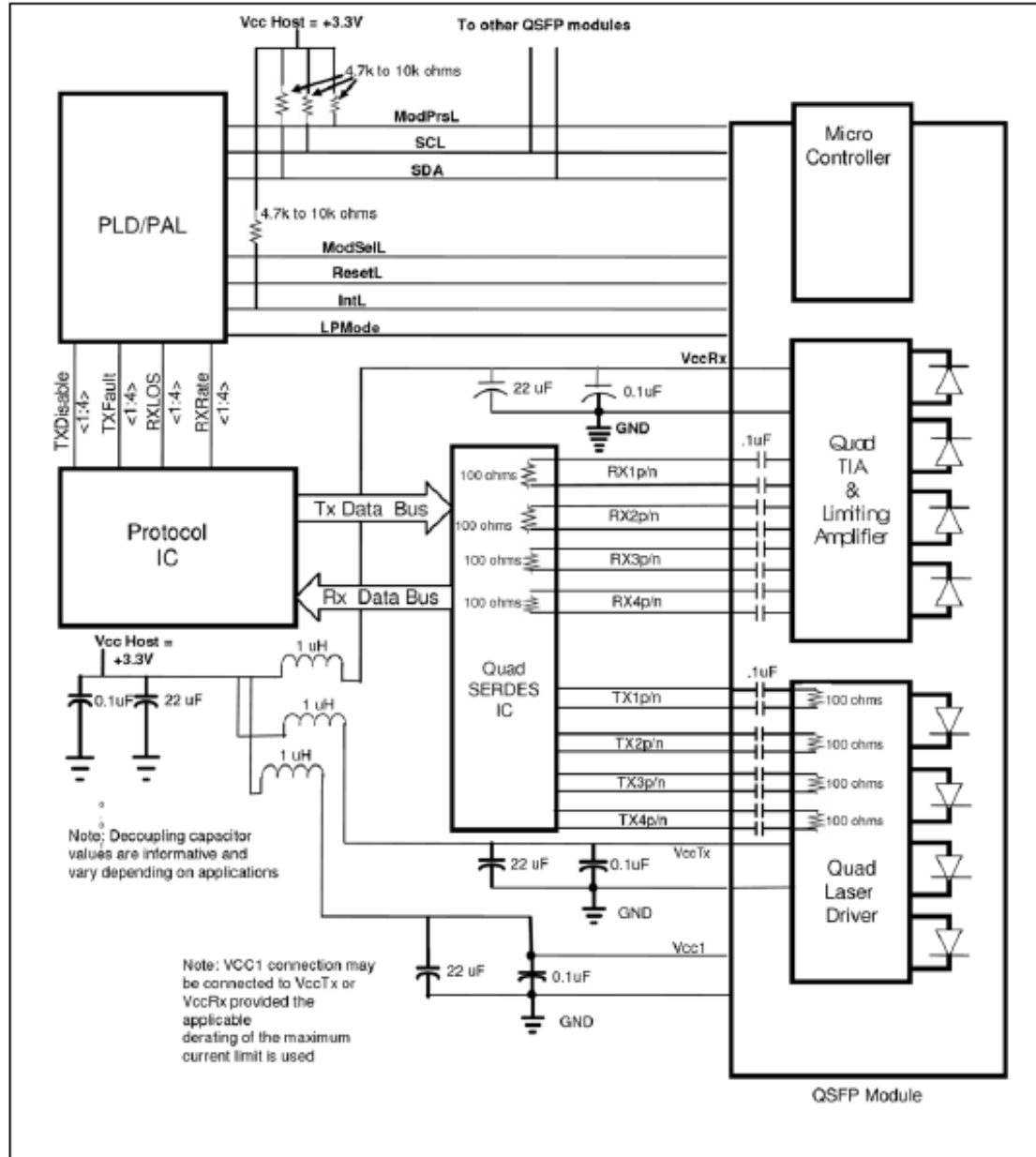
Host board power supply circuit



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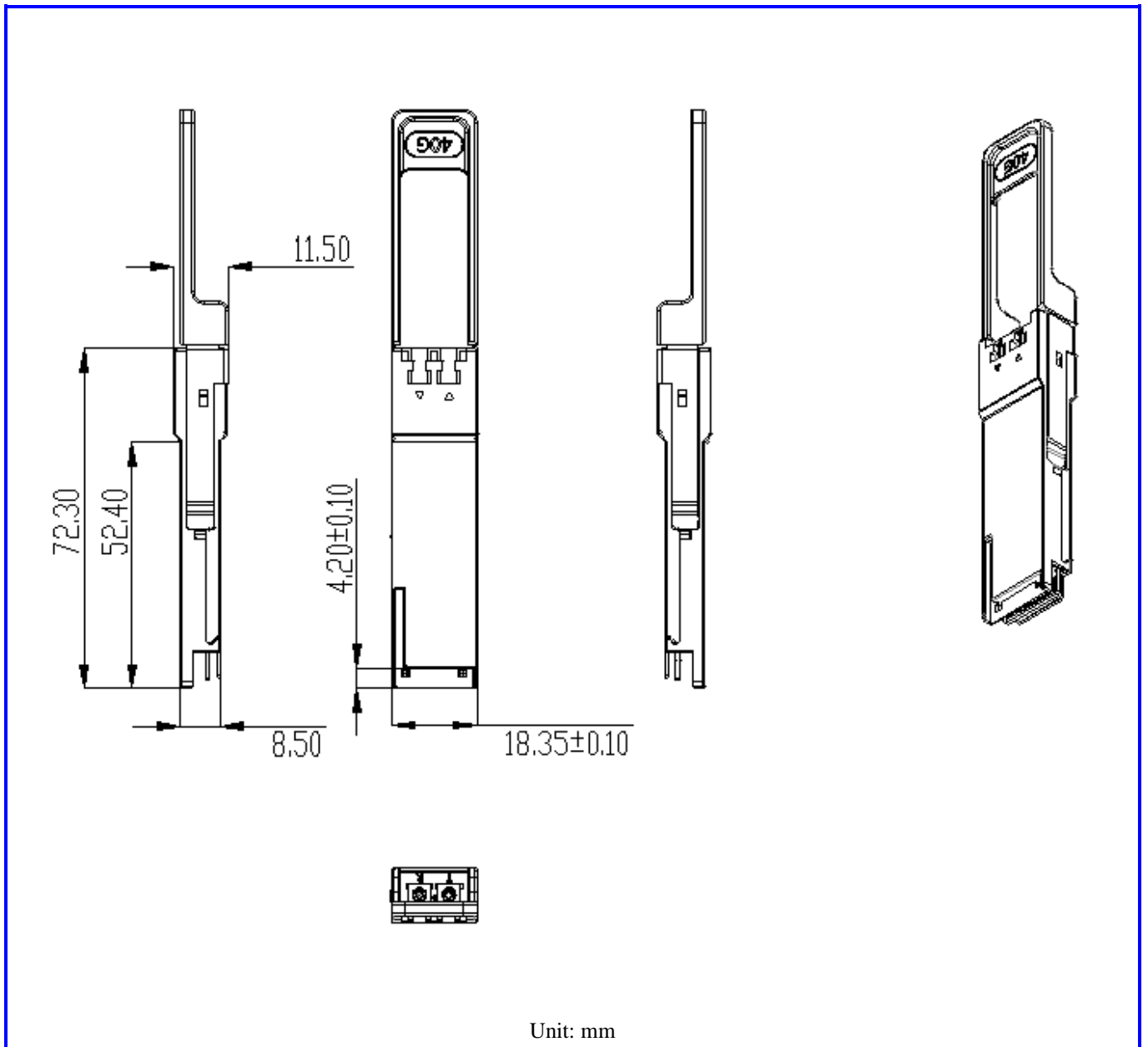
Recommended Interface circuit



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Dimensions



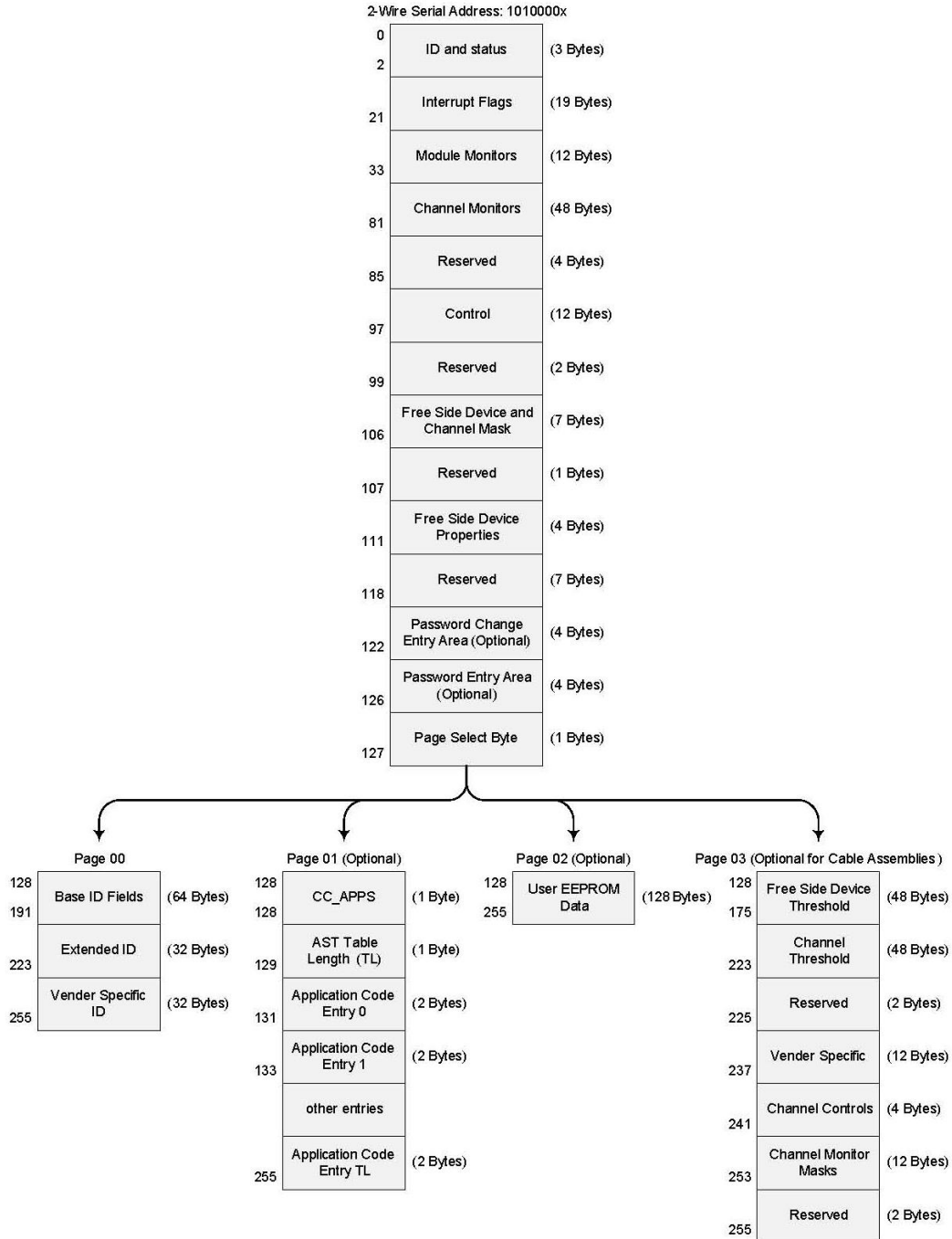


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Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP+ SFF-8436 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.





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Eye Safety Mark

The LS3 series Single-mode transceiver is a class 1 laser product. It complies with EN 60825-1 and FDA 21 CFR 1040.10 and 1040.11. In order to meet laser safety requirements the transceiver shall be operated within the Absolute Maximum Ratings.

Caution

All adjustments have been done at the factory before the shipment of the devices. No maintenance and user serviceable part is required. Tampering with and modifying the performance of the device will result in voided product warranty.

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated (Insert date of this guidance.)

Required Mark

**Class 1 Laser Product
Complies with
21 CFR 1040.10 and 1040.11**

Note : All information contained in this document is subject to change without notice.