Features

- IEEE C37.94 application
- RoHS compliant
- Industry standard 1×9 footprint
- SC duplex connector
- Single power supply 3.3 V
- Differential LVPECL inputs and outputs
- Class 1 laser product complies with EN 60825-1

Ordering Information

PART NUMBER	INPUT/OUTPUT	SIGNAL DETECT	VOLTAGE	TEMPERATURE
LM22-A3S-PC-N-MW	DC/DC	LVPECL	3.3 V	$0\,^{\circ}$C to $70\,^{\circ}$C

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	−40	85	$^{\circ}$C	
Supply Voltage	Vcc	−0.5	4.0	V	
Input Voltage	V_{IN}	−0.5	Vcc	V	
Soldering Temperature	T_{SOLD}	---	260	$^{\circ}$C	10 seconds on leads

Operating Environment

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Case Operating Temperature	T_C	0	70	$^\circ$C	
Supply Voltage	Vcc	3.1	3.5	V	
Power Supply Current(TX+RX)	I_{CC}	---	200	mA	Note1
Data Rate	B	2.048		Mb/s	

Note 1: Not including the terminations current.

Transmitter Electro-optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Output Optical Power 62.5/125μm fiber	P_{out}	-19	---	-11	dBm	Average
Output Optical Power 50/125μm fiber	P_{out}	-23	---	-11	dBm	Average
Extinction Ratio	ER	10	---	---	dB	
Center Wavelength	λ_C	790	---	870	nm	
Transmitter Data Input Voltage-High	$V_{IH} - V_{CC}$	-1.16	---	-0.88	V	
Transmitter Data Input Voltage-Low	$V_{IL} - V_{CC}$	-1.81	---	-1.48	V	

Receiver Electro-optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Optical Input Power-maximum	P_{IN}	-11	---	---	dBm	PRBS7, BER $< 10^{-9}$
Optical Input Power-minimum (Sensitivity)	P_{IN}	---	---	-32	dBm	PRBS7, BER $< 10^{-9}$
Operating Center Wavelength	λ_C	790	---	870	nm	
Signal Detect-Asserted	P_A	---	---	-32	dBm	
Signal Detect-Deasserted	P_D	-45	---	---	dBm	
Signal Detect Output voltage-High	$V_{OH} - V_{CC}$	-1.1	---	-0.74	V	
Signal Detect Output voltage-Low	$V_{OL} - V_{CC}$	-2.0	---	-1.58	V	
Data Output Voltage-High	$V_{OH} - V_{CC}$	-1.1	---	-0.74	V	
Data Output Voltage-Low	$V_{OL} - V_{CC}$	-2.0	---	-1.58	V	

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Block Diagram of Transceiver

ELECTRICAL SUBASSEMBLY

PIN PHOTODIODE

DATA
DATA/

POST AMPLIFIER IC

RRE-AMPLIFIER IC

SIGNAL DETECT

OPTICAL SUB-ASSEMBLIES

DUPLEX SC RECEPTACLE

DATA
DATA/

VCSEL DRIVER IC

VCSEL

TOP VIEW
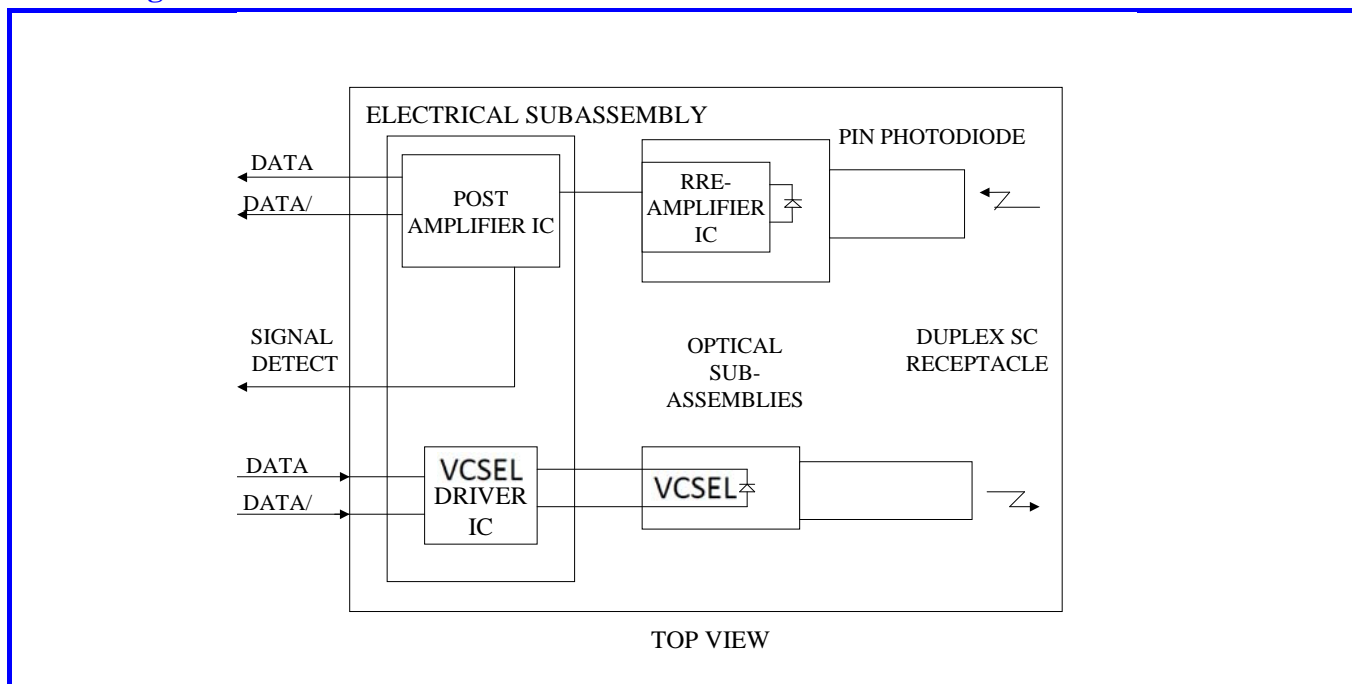
Transmitter Section

The transmitter section consists of a 850 nm VCSEL in an eye safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a LD driver IC which converts differential input LVPECL logic signals into an analog laser driving current.

Receiver Section

The receiver utilizes a PIN photodiode mounted together with a trans-impedance preamplifier IC in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.
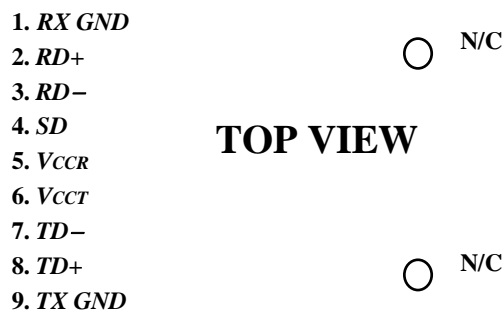
Receiver Signal Detect

Signal Detect is a basic fiber failure indicator. This is a single-ended LVPECL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point).

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Connection Diagram

Pin-Out

1. *RX GND*	○ N/C
2. *RD+*	
3. *RD−*	
4. *SD*	**TOP VIEW**
5. *V_{CCR}*	
6. *V_{CCT}*	
7. *TD−*	
8. *TD+*	○ N/C
9. *TX GND*	

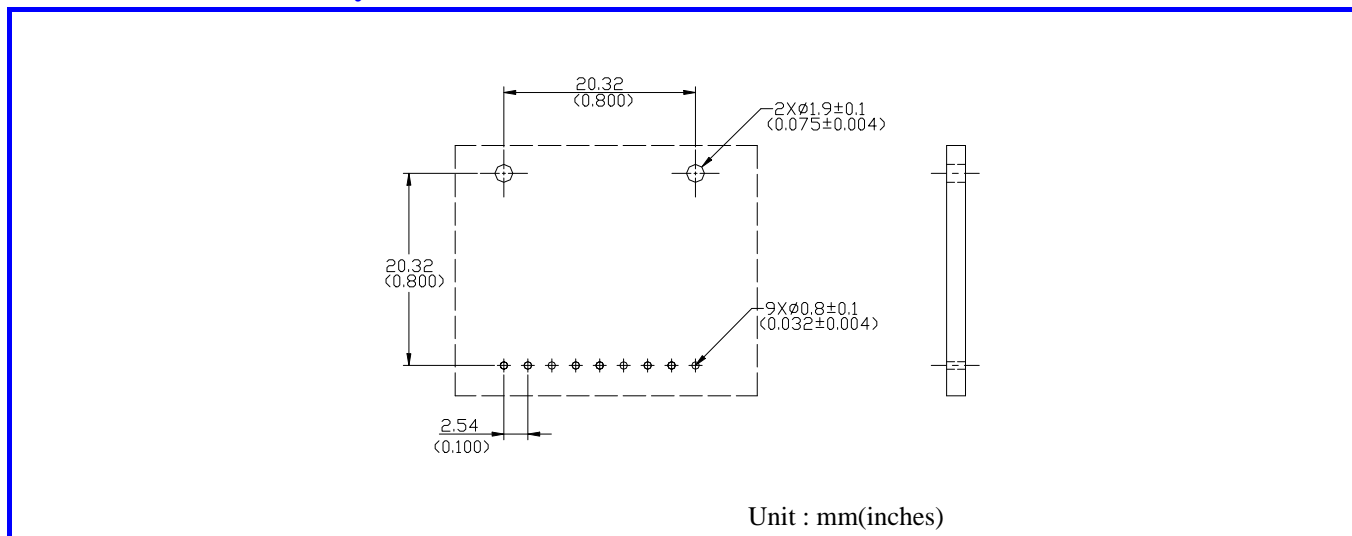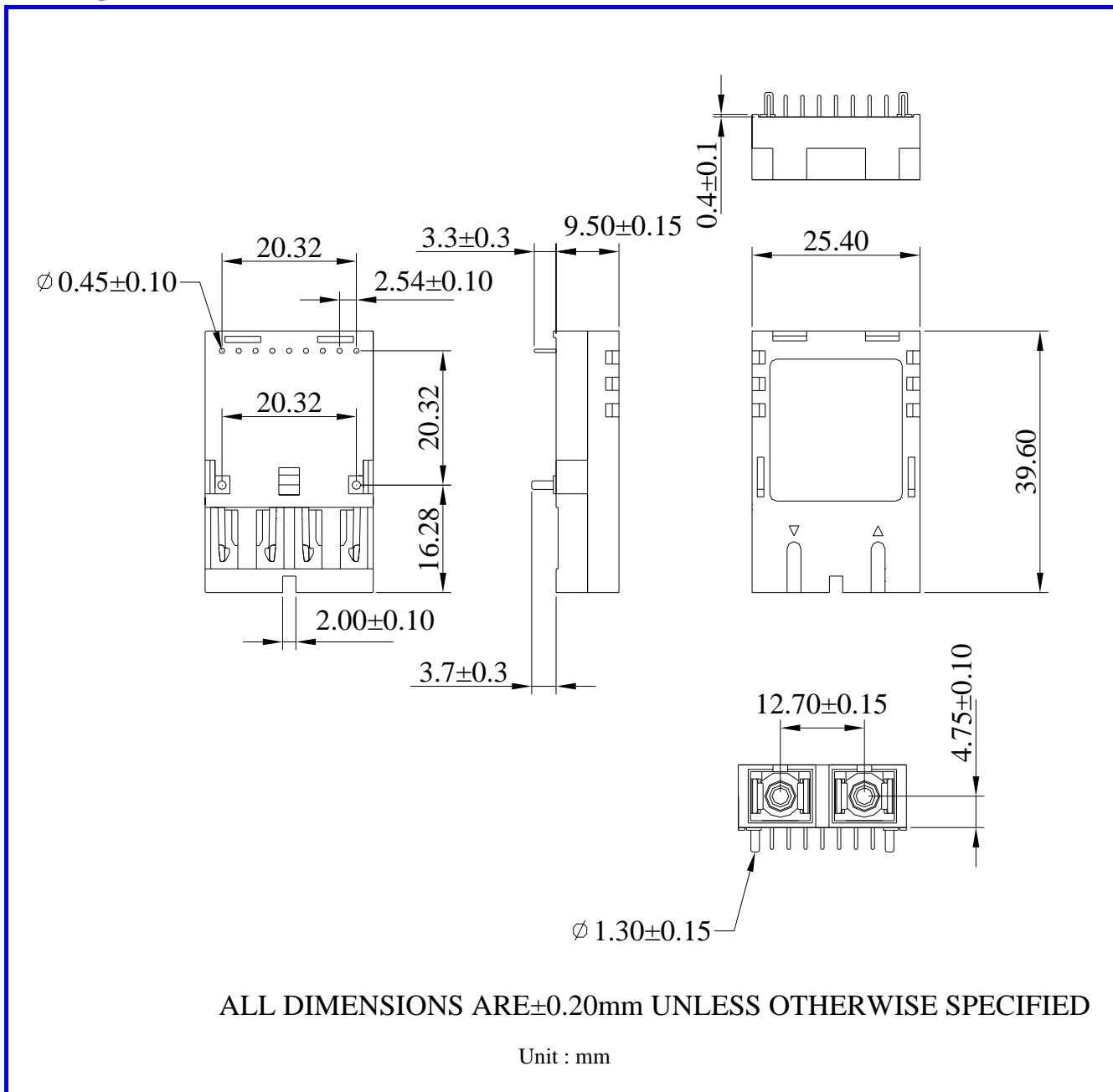| PIN	SYMBOL	DESCRIPTION
1	*RX GND*	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	*RD+*	*RD+* is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
3	*RD−*	*RD−* is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
4	*SD*	Signal Detect. Normal optical input levels to the receiver result in a logic "1" output, V_{OH}, asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic "0" output V_{OL}, deasserted Signal Detect is a single-ended LVPECL output. *SD* can be terminated with LVPECL techniques via 50 Ω to $V_{CCR} - 2$ V. Alternatively, *SD* can be loaded with a 180 Ω resistor to *RX GND* to conserve electrical power with small compromise to signal quality. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a LVPECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
5	*V_{CCR}*	Receiver Power Supply. Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	*V_{CCT}*	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	*TD−*	Transmitter Data In-Bar. Terminate this high-speed differential LVPECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)
8	*TD+*	Transmitter Data In. Terminate this high-speed differential LVPECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)
9	*TX GND*	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.

Recommended Circuit Schematic

DC/DC Coupling

$C1/C2/C4 = 0.1 \ \mu F$
$L1/L2 = 1 \ \mu H$
$R1/R3/R5/R7/R9 = 130 \ \Omega$

$C3 = 4.7 \ \mu F$

$R2/R4/R6/R8/R10 = 82 \ \Omega$
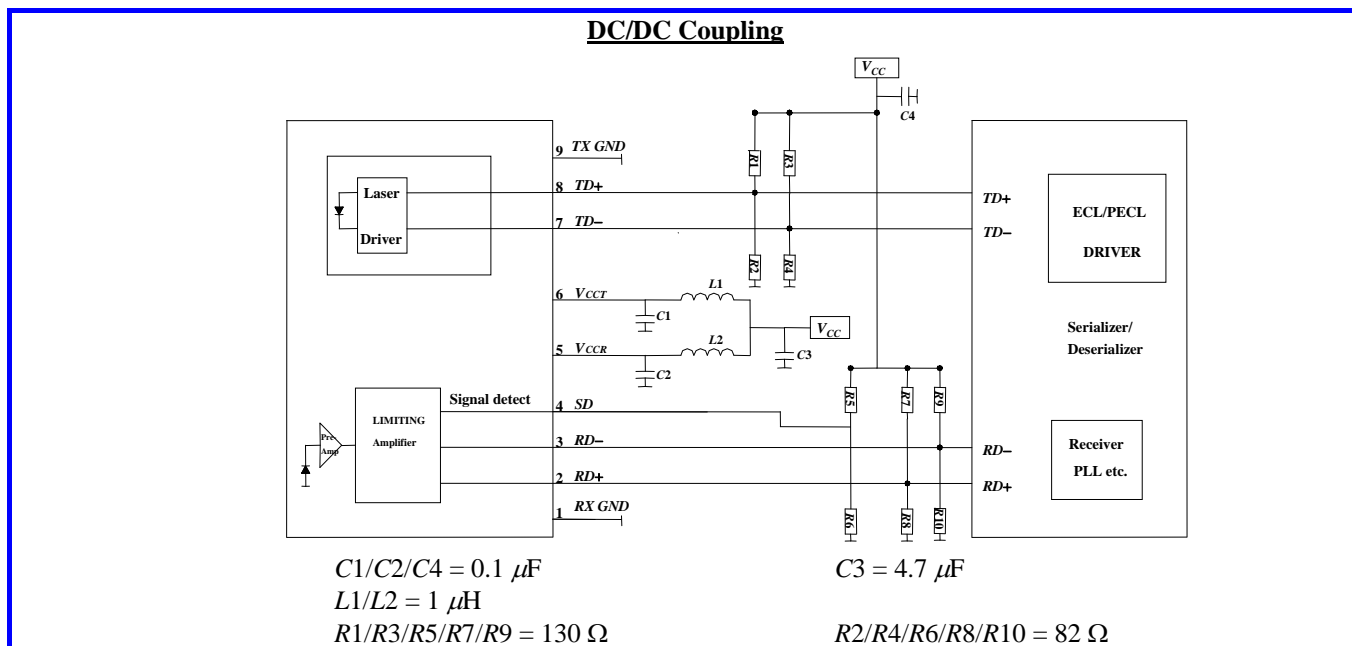
Recommended Board Layout Hole Pattern

20.32
(0.800)

2XØ1.9±0.1
(0.075±0.004)

20.32
(0.800)

9XØ0.8±0.1
(0.032±0.004)

2.54
(0.100)

Unit : mm(inches)

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Drawing Dimensions

ALL DIMENSIONS ARE±0.20mm UNLESS OTHERWISE SPECIFIED

Unit : mm

Note : All information contained in this document is subject to change without notice.