QSFP+ 40Gbps PSM4 Transceiver

Compliance with 10GBASE-LR for up to 10km reach

Description

APAC QSFP+PSM4 transceiver is a new high speed module with a MPO connector. This interconnecting module offers 4 channels and maximum bandwidth of 40Gbps. The module consist 4x10Gbps 1310nm DFB LDs transmitter and 4x10G PINs receiver.

Features

- Supports 4x10GBASE-LR
- Power dissipation < 3.5W with single 3.3V power supply
- Full Digital Diagnostics Monitor Interface
- Up to 10km transmission on SMF
- RoHS-6 Compliant (lead-free)
- MPO12 receptacle

Application

- 4x10GBASE-LR/LW
- Data Center Interconnects

Ordering information

PART NUMBER	DISTANCE	TEMPERATURE	NOTE
LS3C-K3S-TC-N-AK	10 km	0°C to 70 °C	4X10Gbps

Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	-40	85	°C	
Power Supply Voltage	Vcc	–0.5	3.6	V	
Relative Humidity	RH	5	85	%	

Recommend Operating Condition

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Case Temperature	Tc	0		70	°C	
Power Supply Voltage	Vcc	3.14	3.3	3.47	V	
Power Dissipation				2.5	W	

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Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Module internal Temperature	-5 to 75	± 3	°C	Internal
Module internal Voltage	3.0 to 3.6	± 0.1	V	
Bias Current	0 to 100	± 10%	mA	
TX Power	-5 to +6	± 3 dB	dBm	
RX Power	-24 to 0	± 3 dB	dBm	

Transmitter Optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Average Output Power, per Lan	Po	-8.2		+0.5	dBm	
Optical Modulation Amplitude, per lane	POMA	-5.2		+2	dBm	
Extinction Ratio	ER	3.5			dB	
Center Wavelength	λc	1260		1360	nm	
Side Mode Suppression	SMSR	30			dB	
Relative Intensity Noise	RIN20OMA			-128	dB/Hz	
Optical Return Loss	ORL			-12	dB	
Transmitter and Dispersion Penalty	TDP			2.3	dB	
Output Eye Mask	Compliant with IEEE 802.3ba					
Disable Output Power	Po_off			-30	dBm	
Differential Input Swing		200		800	mV	

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Receiver Optical characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Damage Threshold, per lane	Pth	3.3			dBm	
Average power at receiver input, per Lane		-14.2		0.5	dBm	
Receiver Power (OMA), per Lane				+0.5	dBm	
Receiver Sensitivity (OMA), per Lane	Rsens			-12.6	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-15	dBm	
Hysteresis	Hys	0.5		6	dB	
Differential Output Swing		400		850	mV	

Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate, per lane			10.3125		Gbps	
LP Mode/Reset/ModselL	VIL	0		0.8	V	
LP Mode/Reset/ModselL	VIH	2		Vcc+0.3	V	
ModPrsL/IntL	VOL	0		0.4	V	
ModPrsL/IntL	VOH	2		Vcc+0.3	V	

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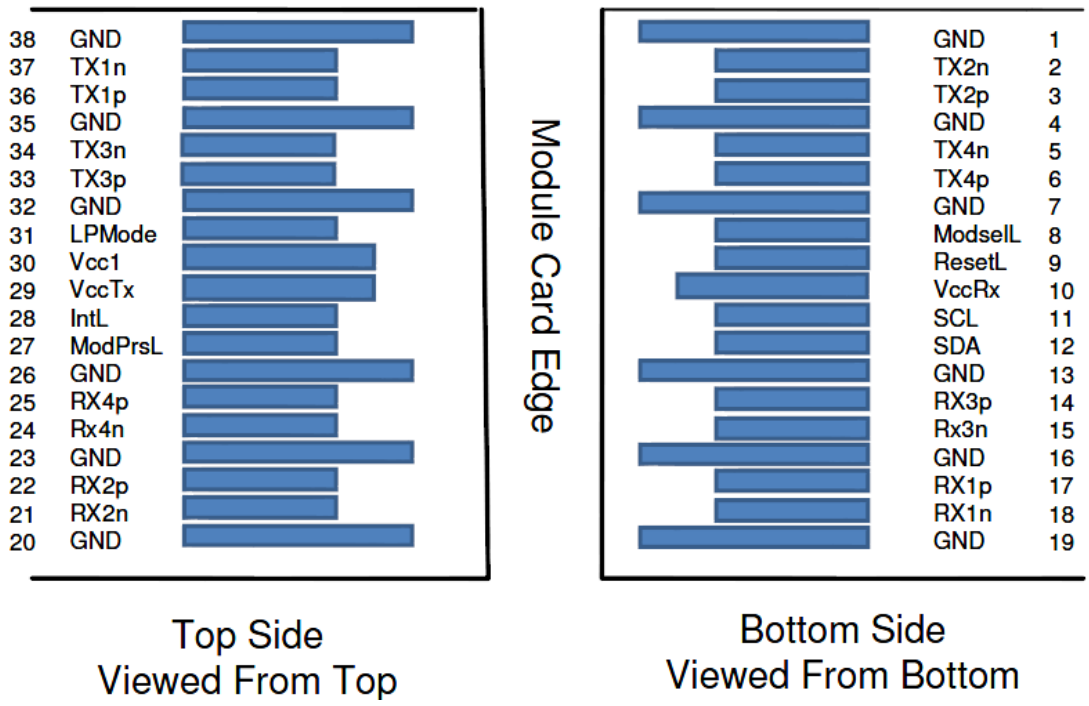
Pad assignment and Description



"PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
1		GND	Ground	1	Note 1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	Note 1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	Note 1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	Note 2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	Note 2
14	CML-O	Rx3p	Receiver Non- Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	Note 1
17	CML-O	Rx1p	Receiver Non- Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	Note 1
20		GND	Ground	1	Note 1

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21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2P	Receiver Non- Inverted Data Output	3	
23		GND	Ground	1	Note 1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non- Inverted Data Output	3	
26		GND	Ground	1	Note 1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29	LVCMOS-I/O	Vcc Tx	+3.3V Power Supply transmitter	2	Note 2
30		Vcc1	+3.3V Power Supply	2	Note 2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	Note 1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	Note 1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	Note 1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

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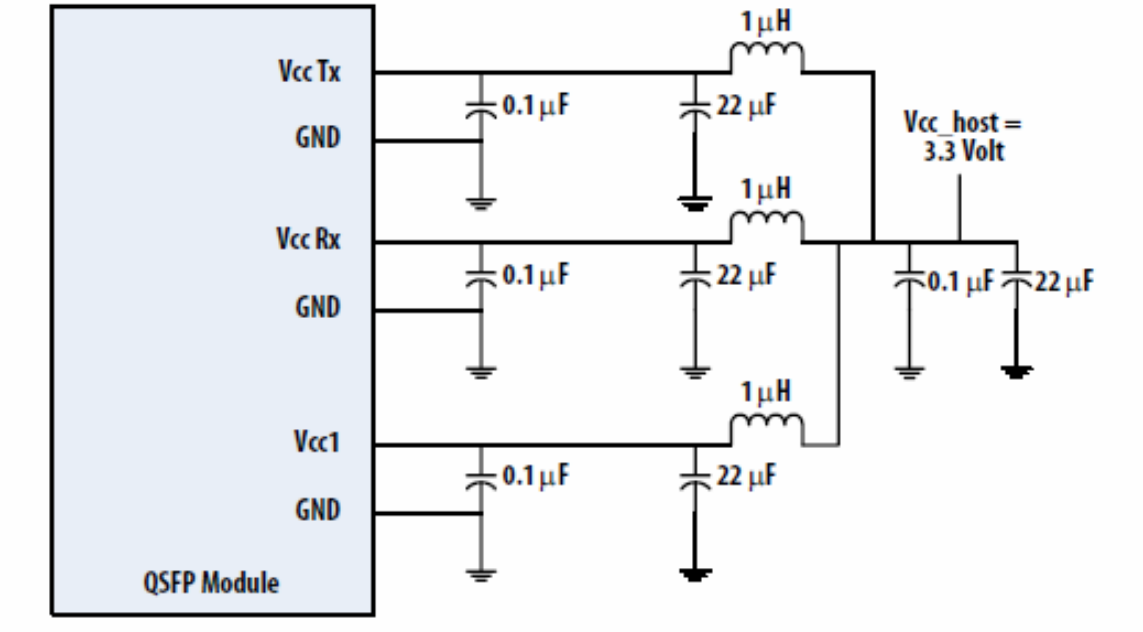
Host board power supply circuit



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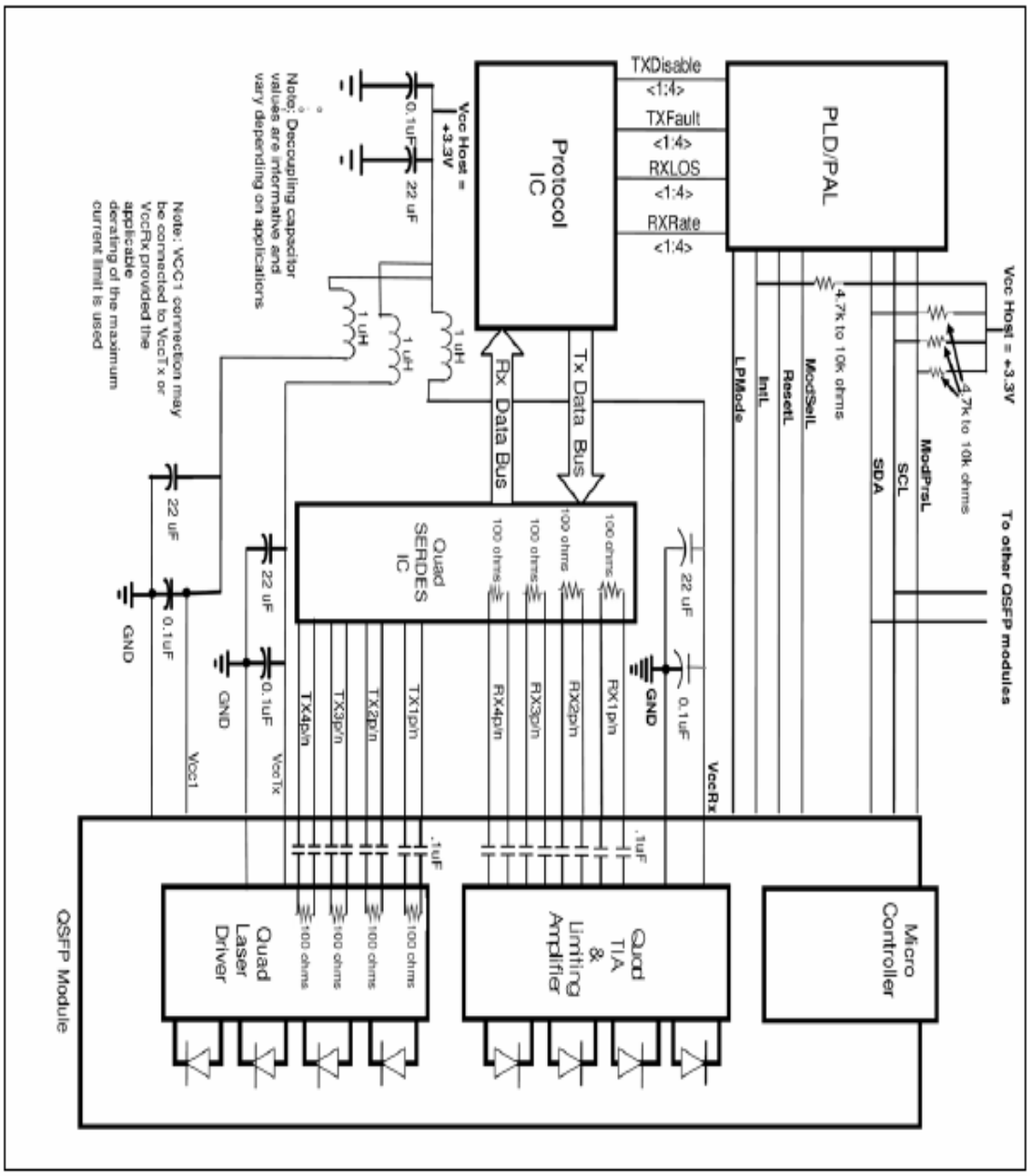
Recommended Interface circuit



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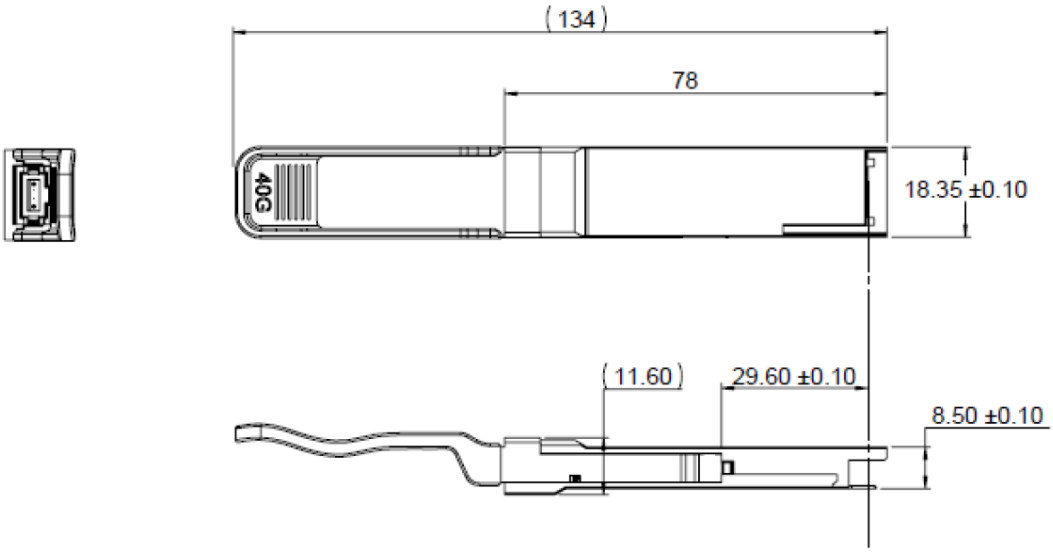
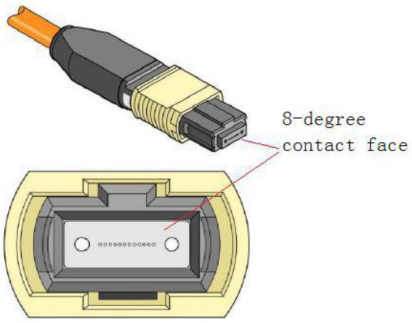
Dimensions



Unit: mm

Attention: To minimize MPO connection induced reflections, an MPO receptacle with 8-degree angled end-face is utilized for this product. A male MPO connector with 8-degree end-face should be used with this product as illustrated in below.



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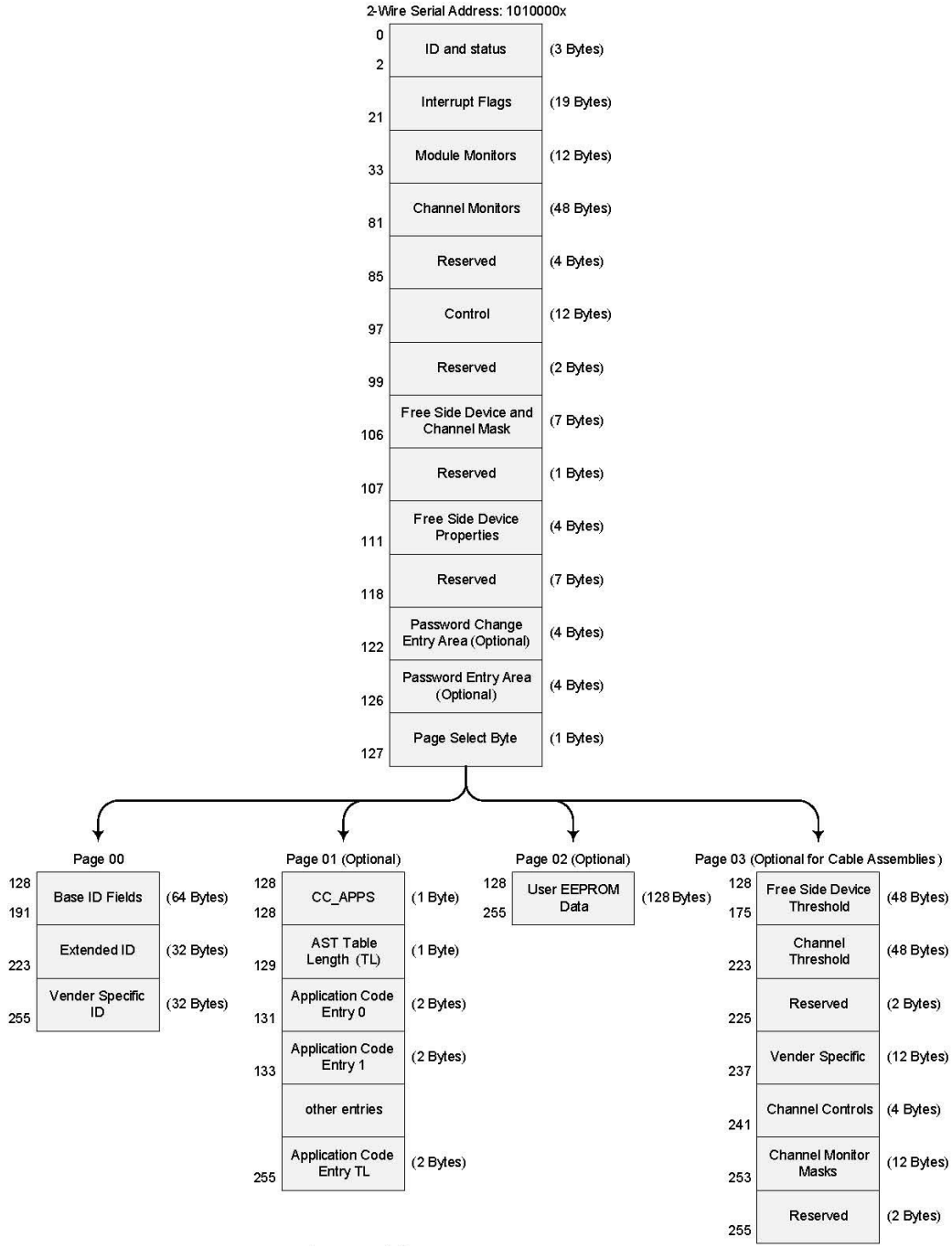
Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP+ SFF-8436 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



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