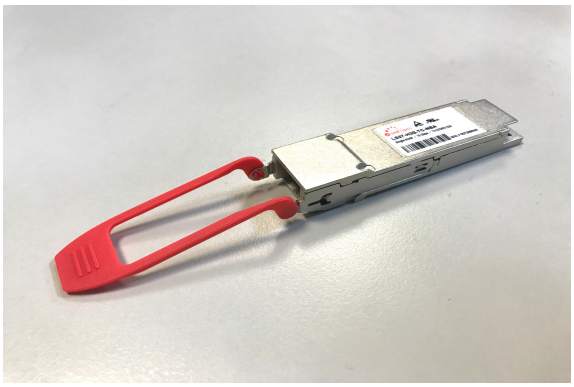
QSFP28 100G-ER4 Lite Transceiver

Multi rate support 100GBASE Ethernet and OTU4 Application
1310nm LAN WDM



Description

APAC QSFP28 transceiver modules are designed for use in 100 Gigabit Ethernet links on up to 30 km of single mode fiber .Digital diagnostics functions are available via the I2C interface, as specified by the QSFP28 MSA.

Features

- Hot-pluggable QSFP28 form factor
- Power dissipation < 4.5W
- Single 3.3V power supply
- RoHS-6 Compliant (lead-free)
- Case temperature range of 0°C to +70°C
- 4x28 Gb/s EML laser and APD photo diode
- 4x28G retimed electrical interface
- Duplex LC receptacles
- I2C management interface
- Up to 30km reach for G.652 SMF without FEC
- Up to 40km reach for G.652 SMF with FEC
- Supports 103.1Gb/s and 112Gb/s bit rate

Application

- 100G Ethernet
- Data Center Interconnects
- OTN OTU4

Ordering information

PART NUMBER	DISTANCE	TEMPERATURE	NOTE
LS3C-L3L-TC-N-DR	30 km	0°C to 70 °C	4X28Gbps

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Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	-40	85	°C	
Power Supply Voltage	Vcc	–0.5	3.6	V	
Relative Humidity	RH	5	85	%	

Recommend Operating Condition

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Case Temperature	Tc	0		70	°C	
Power Supply Voltage	Vcc	3.14	3.3	3.46	V	
Power Dissipation				4.5	W	

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Transmitter Optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Operating Data Rate	*DR*	25.78125		27.9525	Gbps	
Total Average Launch Power	*Pt*			10.5	dBm	
Average Launch Power, per Lane		-2.9		4.5	dBm	
Extinction Ratio	*ER*	6.5			dB	
Optical Modulation Amplitude, per lane	*Poma*	-0.5			dBm	
Transmitter Dispersion Penalty, each Lane	*TDP*			2.5	dB	
Center Wavelength	*L0*	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Side Mode Suppression	*SMSR*	30			dB	
Transmitter Reflectance	*RT*			-12	dB	
Disable Output Power	*Po_off*			-30	dBm	
Output Eye Mask Definition {X1, X2, X3,Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				

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Receiver Optical characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Damage Threshold, per lane	Pth	-4			dBm	
Receiver Sensitivity(OMA), per lane (BER= $5X10^{-5}$)	Sen1			-18.7	dBm	@25.78Gbps
Receiver Sensitivity(OMA), per lane (BER= $1X10^{-12}$)	Sen2			-14.7	dBm	
Stressed Receiver Sensitivity in OMA, per lane(BER= $5X10^{-5}$)	Sen3			-16.7	dBm	
Receiver Sensitivity(OMA), per lane (BER= $5X10^{-5}$)	Sen4			-18	dBm	@27.95Gbps, Note1
Receiver reflectance	RR			-26.0	dB	
LOS De-Assert	LOSD		-24		dBm	
LOS Assert	LOSA		-26		dBm	
LOS Hysteresis		0.5			dB	

Note1: Tested with a $2^{31} – 1$ PRBS. Per ITU-T G.959.1 and G.sup39, the BER of 10^{-12} for the OTU4 application code is required to be met only after forward error correction has been applied. ITU-T G.sup39 defines the pre-FEC BER to be met as $5x10^{-5}$. The values for receiver sensitivity and optical path penalty measured at the receiver output at a BER of $5x10^{-5}$ will normally be conservative estimates of the values for receiver sensitivity and path penalty at the BER of 10^{-12} after the FEC decoder.

Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
LP Mode/Reset/ModselL	VIL	-0.3		0.8	V	
LP Mode/Reset/ModselL	VIH	2		Vcc+0.3	V	
ModPrsL/IntL	VOL	0		0.4	V	
ModPrsL/IntL	VOH	Vcc-0.5		Vcc+0.3	V	

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Rate select description

When (Page 00h Byte 221 bits 2 and 3) have the values of 0 and 1 respectively and at least one of the bits in the Extended Rate Compliance byte (Page 00h Byte 141 bit 1) have a value of one, the free side device supports extended rate select. For extended rate selection, two bits are assigned to each receiver in Byte 87 (Rxn_Rate_Select) and two bits for each transmitter in Byte 88 (Txn_Rate_Select) to specify up to four bit rates. See Table 1 for the functionality when Byte 141 bits 0-1 are set. All other values of the Extended Rate Compliance byte are reserved.

Table 1 T/RxN_RATE_SELECT WITH EXTENDED RATE SELECTION

Page 00h Byte 141 Bit 1 = 1		
T/RxN_Rate_Select (MSB Value)	T/RxN_Rate_Select (LSB Value)	Description
0	0	Operation at the 25.78Gbps
0	1	
1	0	
1	1	Operation at the 27.95Gbps

Table 2 Page 00h Byte 87 and 88 rate select register define

Addr(DEC)	Addr(HEX)	Name of Field	BIT	Name
87	0x57h	Rx Rate select register	7	Rx4_Rate_Select MSB
			6	Rx4_Rate_Select LSB
			5	Rx3_Rate_Select MSB
			4	Rx3_Rate_Select LSB
			3	Rx2_Rate_Select MSB
			2	Rx2_Rate_Select LSB
			1	Rx1_Rate_Select MSB
			0	Rx1_Rate_Select LSB
88	0x58h	Tx Rate select register	7	Tx4_Rate_Select MSB
			6	Tx4_Rate_Select LSB
			5	Tx3_Rate_Select MSB
			4	Tx3_Rate_Select LSB
			3	Tx2_Rate_Select MSB
			2	Tx2_Rate_Select LSB
			1	Tx1_Rate_Select MSB
			0	Tx1_Rate_Select LSB

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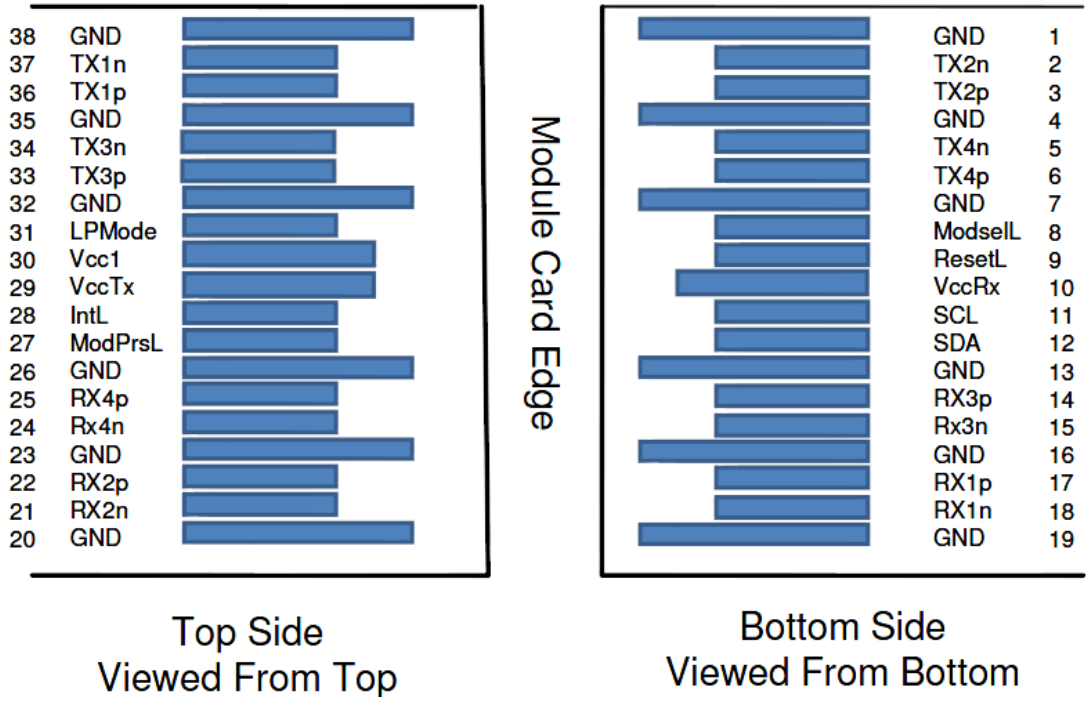
Pad assignment and description



PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
1		GND	Ground	1	Note 1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	Note 1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	Note 1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	Note 2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	Note 2
14	CML-O	Rx3p	Receiver Non- Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	Note 1
17	CML-O	Rx1p	Receiver Non- Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	Note 1
20		GND	Ground	1	Note 1

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21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2P	Receiver Non- Inverted Data Output	3	
23		GND	Ground	1	Note 1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non- Inverted Data Output	3	
26		GND	Ground	1	Note 1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29	LVCMOS-I/O	Vcc Tx	+3.3V Power Supply transmitter	2	Note 2
30		Vcc1	+3.3V Power Supply	2	Note 2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	Note 1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	Note 1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	Note 1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP module in any combination. The connector pins are each rated for a maximum current of 500 mA.

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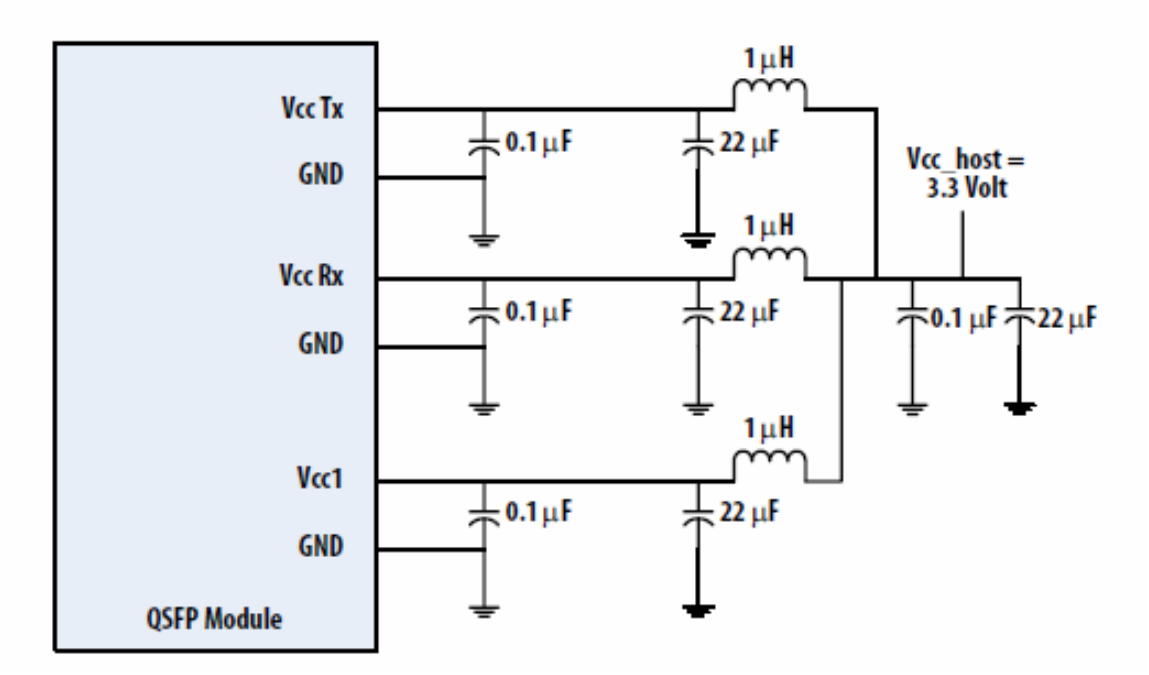
Host board power supply circuit



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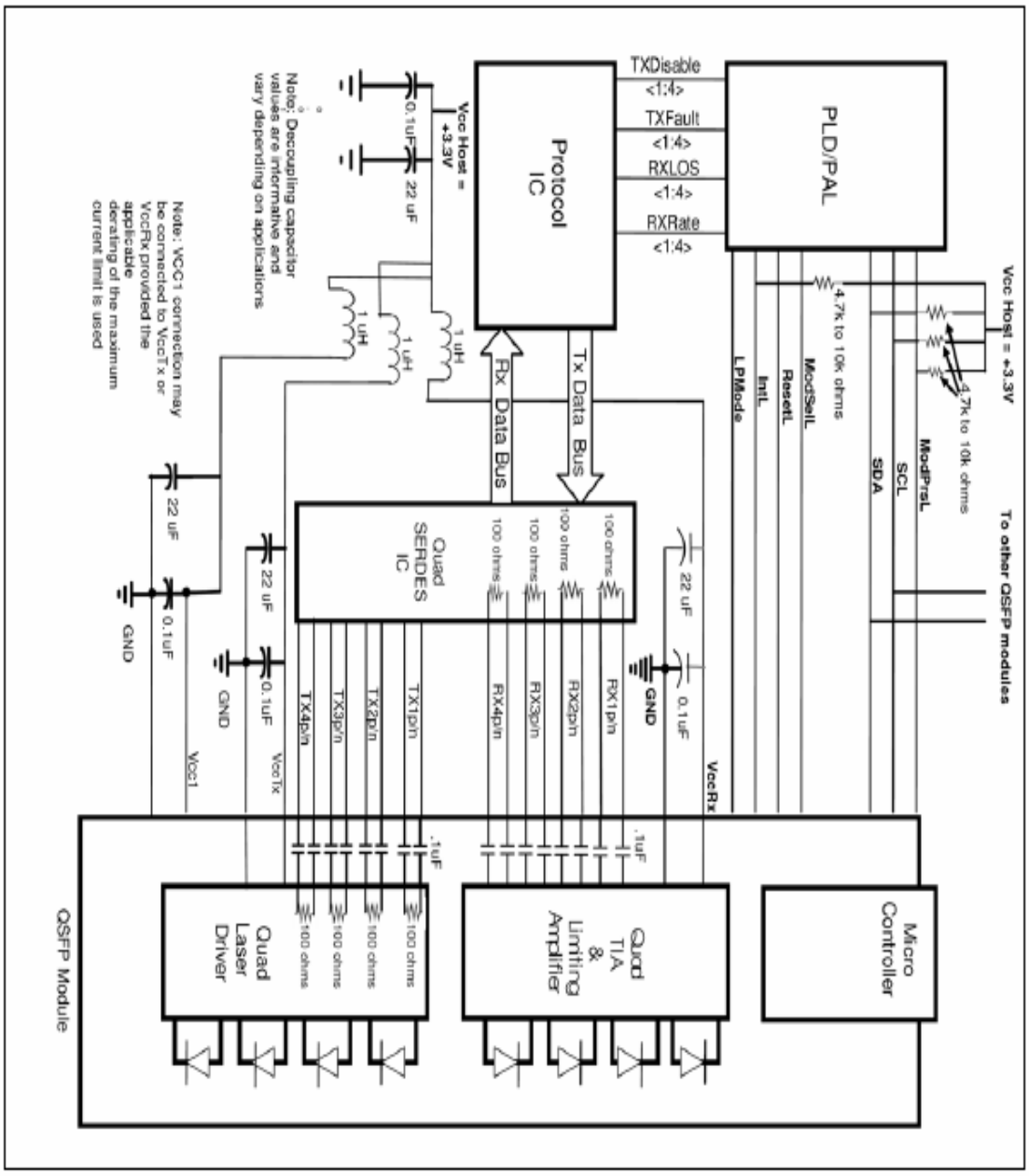
Recommended Interface circuit



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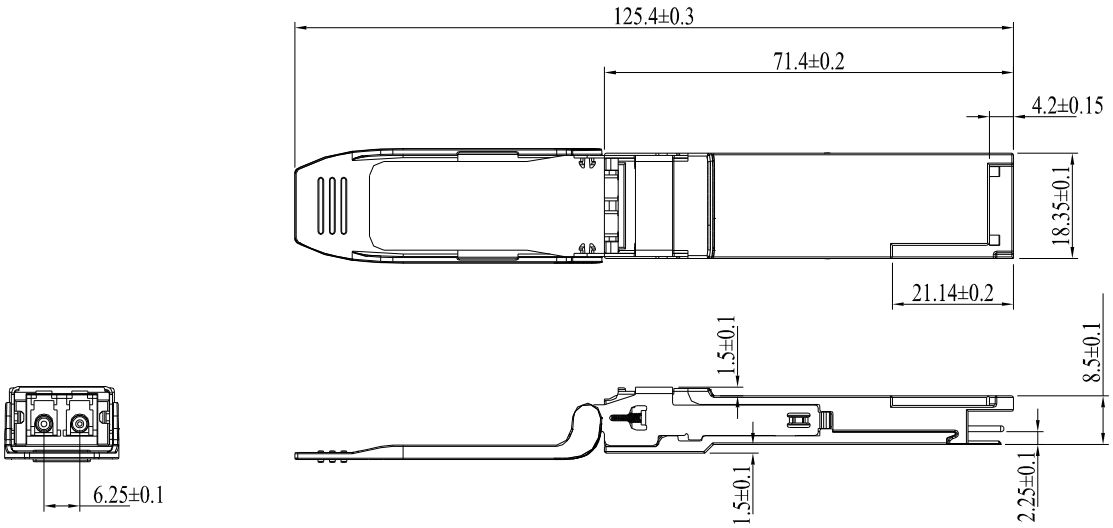
Dimensions



Unit: mm

All Dimensions are ±0.20mm Unless Otherwise Specified

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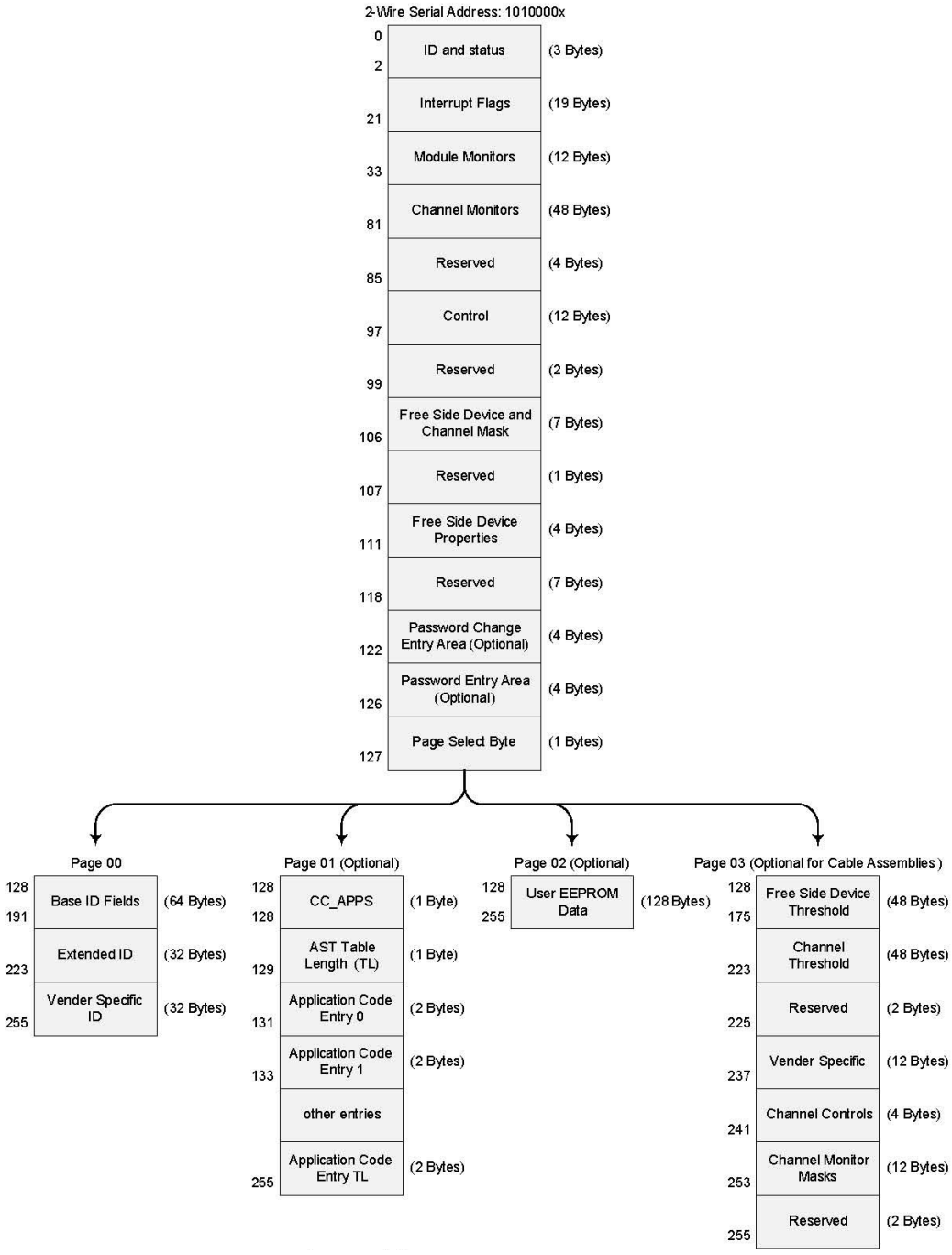
Memory Map



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