

### Features

- Hot-pluggable QSFP28 form factor
- Power dissipation < 5.5W
- Single 3.3V power supply
- RoHS Compliant (lead-free)
- Case temperature range of 0°C to +70°C
- 4x28 Gb/s EML integrated TOSA
- 4x28 Gb/s PIN+SOA ROSA
- 4x28G retimed electrical interface
- Duplex LC receptacles
- I2C management interface

### Description

APAC QSFP28 transceiver modules are designed for use in 100 Gigabit Ethernet links on up to 80 km of single mode fiber .Digital diagnostics functions are available via the I2C interface, as specified by the QSFP28 MSA.

### Application

- 100G Ethernet
- Data Center Interconnects
- OTU4

### Ordering information

PART NUMBER	DISTANCE	TEMPERATURE	NOTE
LS3C-L3U-TC-N-DR	80 km	0° C to 70° C	4X28Gbps

**Note: Attenuation of 0.35 dB/km @1310nm is used for the link length calculations**

### Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	$T_S$	-40	85	°C	
Power Supply Voltage	$V_{cc}$	-0.5	3.6	V	
Relative Humidity	$RH$	5	85	%	



# QSFP28 100GBASE-ZR4 Transceiver

1310nm LAN WDM up to 80km reach

## Recommend Operating Condition

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Case Temperature	$T_c$	0		70	°C	
Power Supply Voltage	$V_{cc}$	3.14	3.3	3.46	V	
Power Dissipation				5.5	W	@3.3V

## Transmitter Optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE	
<b>L</b>							
Operating Data Rate	$DR$		25.78125	28	Gbps		
Total Average Launch Power	$P_t$	8		12.5	dBm	(1)	
Average Launch Power, per lane		2		6.5	dBm		
Optical Modulation Amplitude, per lane	$P_{oma}$	3		7.5	dBm		
Extinction Ratio	$ER$	7			dB		
Difference in Launch Power between any Two Lanes (OMA)	$P_{tx, diff}$			3.6	dBm		
Transmitter Dispersion Penalty, per lane	$TDP$			1	dB		
Center Wavelength	$L0$	1294.53	1295.56	1296.59	nm		
	$L1$	1299.02	1300.05	1301.09	nm		
	$L2$	1303.54	1304.58	1305.63	nm		
	$L3$	1308.09	1309.14	1310.19	nm		
Side Mode Suppression	$SMSR$	30			dB		
RIN <sub>20OMA</sub>	$RIN$			-130	dB/Hz		
Optical Return Loss Tolerance	$TOL$			20	dB		
Transmitter Reflectance	$RT$			-12	dB		
Disable Output Power	$P_{o\_off}$			-30	dBm		
Output Eye Mask Definition { X1, X2, X3, Y1, Y2, Y3 }		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					



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## Receiver Optical characteristics

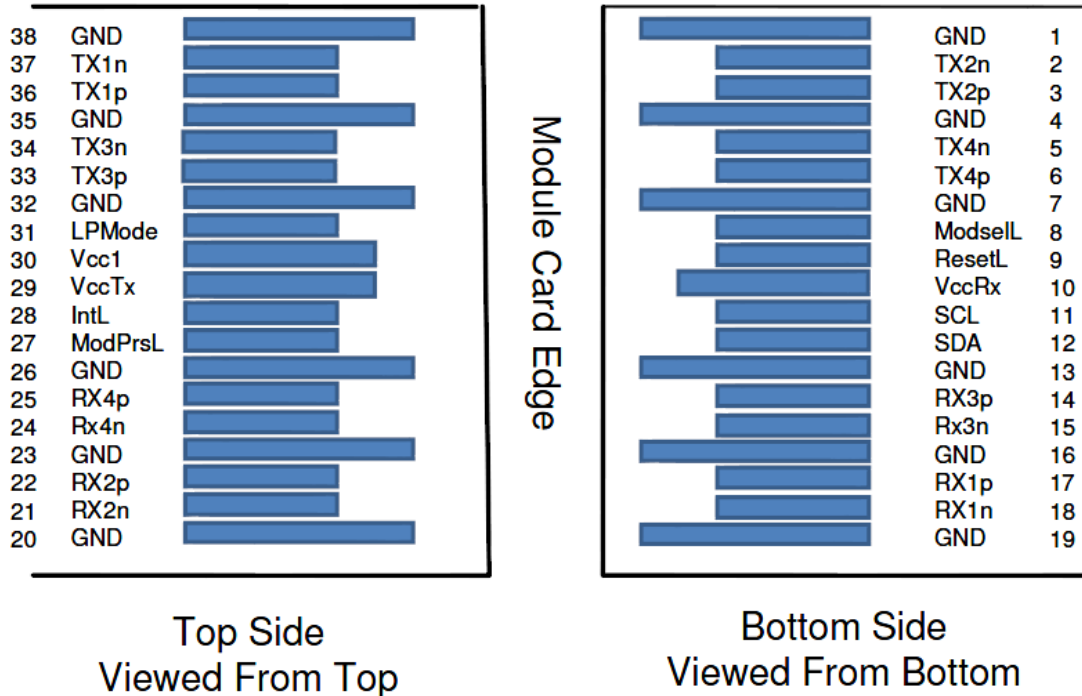
PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Damage Threshold, per lane	<i>P<sub>th</sub></i>	4.5			dBm	
Average Receiver Power , per lane		-28		-7	dBm	(1)
Average Receiver Sensitivity , per lane	<i>S<sub>en</sub></i>			-28	dBm	BER = 5X10 <sup>-5</sup> with FEC
Receiver reflectance	<i>RR</i>			-26	dB	
Receiver Electrical 3dB upper Cutoff Frequency, per lane	<i>F<sub>c</sub></i>			31	GHz	
LOS De-Assert	<i>LOSD</i>			-30	dBm	
LOS Assert	<i>LOSA</i>	-40			dBm	
LOS Hysteresis		0.5			dB	

Note1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

## Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate, per lane			25.78125	28	Gbps	
LP Mode/Reset/ModselL	<i>V<sub>IL</sub></i>	-0.3		0.8	V	
LP Mode/Reset/ModselL	<i>V<sub>IH</sub></i>	2		V <sub>cc</sub> +0.3	V	
ModPrsL/IntL	<i>V<sub>OL</sub></i>	0		0.4	V	
ModPrsL/IntL	<i>V<sub>OH</sub></i>	V <sub>cc</sub> -0.5		V <sub>cc</sub> +0.3	V	

## Pad assignment and Description



PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
1		GND	Ground	1	Note 1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	Note 1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	Note 1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	Note 2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	Note 2
14	CML-O	Rx3p	Receiver Non- Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	Note 1
17	CML-O	Rx1p	Receiver Non- Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	Note 1
20		GND	Ground	1	Note 1



# QSFP28 100GBASE-ZR4 Transceiver

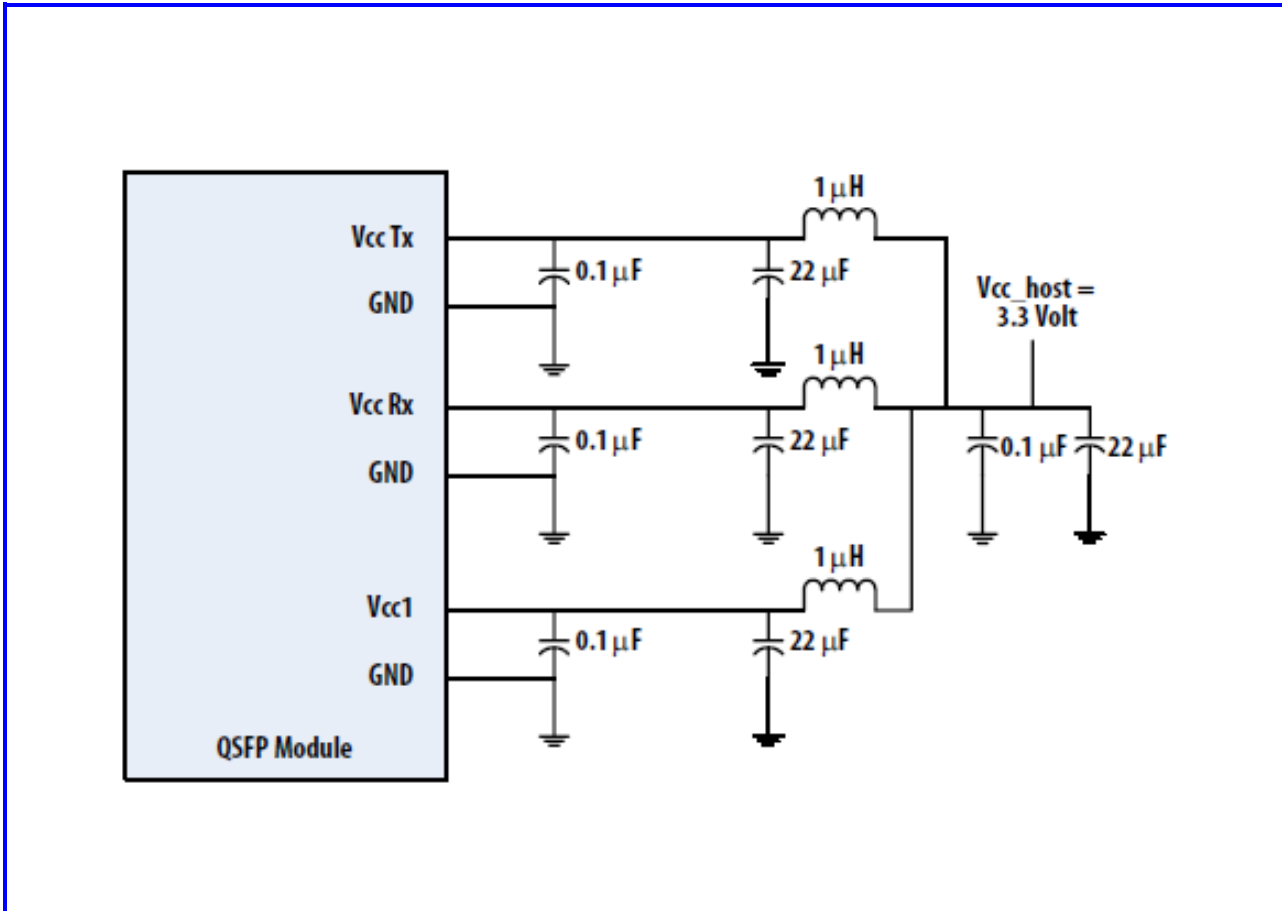
1310nm LAN WDM up to 80km reach

21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2P	Receiver Non- Inverted Data Output	3	
23		GND	Ground	1	Note 1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non- Inverted Data Output	3	
26		GND	Ground	1	Note 1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29	LVC MOS-I/O	Vcc Tx	+3.3V Power Supply transmitter	2	Note 2
30		Vcc1	+3.3V Power Supply	2	Note 2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	Note 1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	Note 1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	Note 1

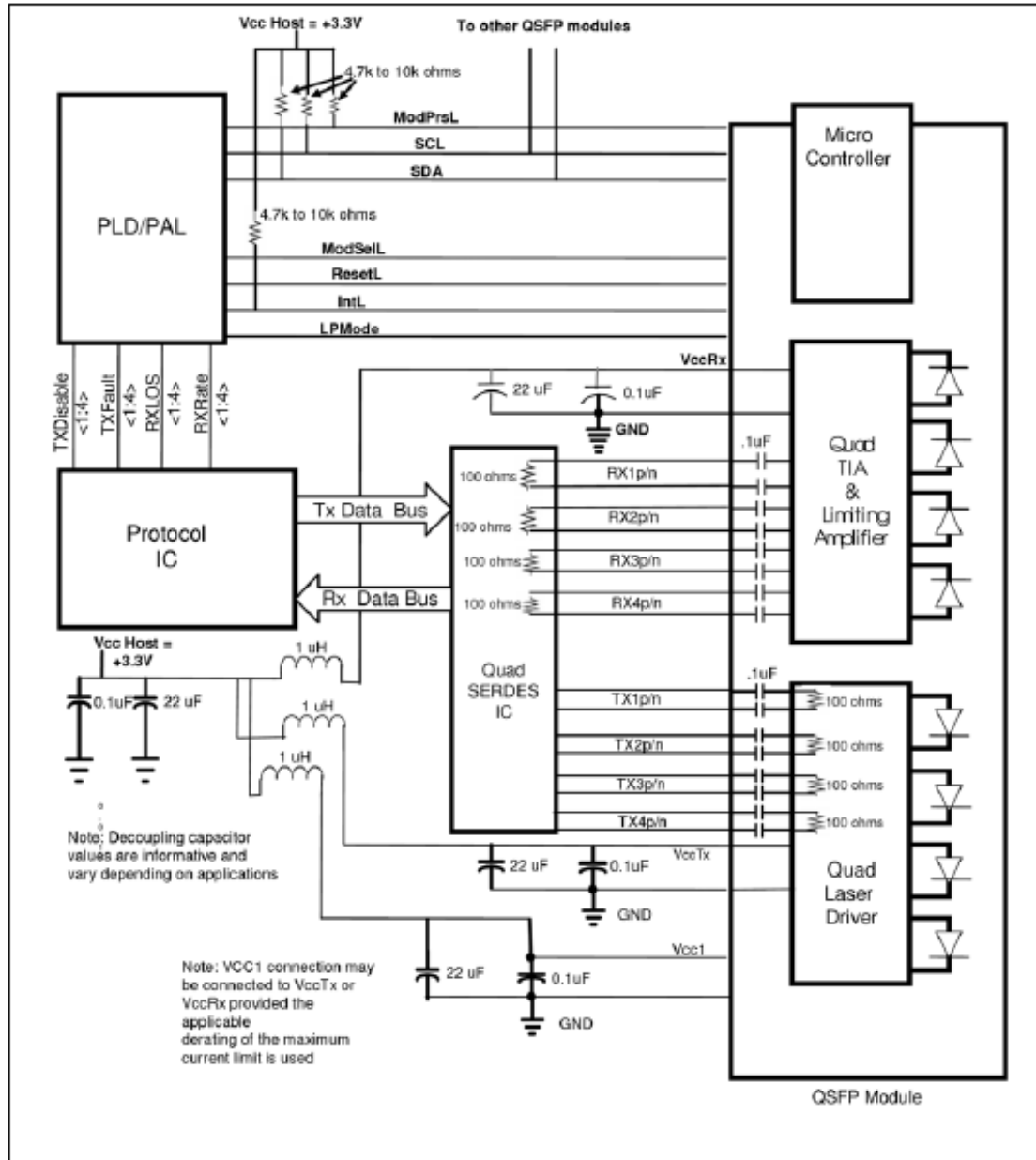
Note 1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP module in any combination. The connector pins are each rated for a maximum current of 500 mA.

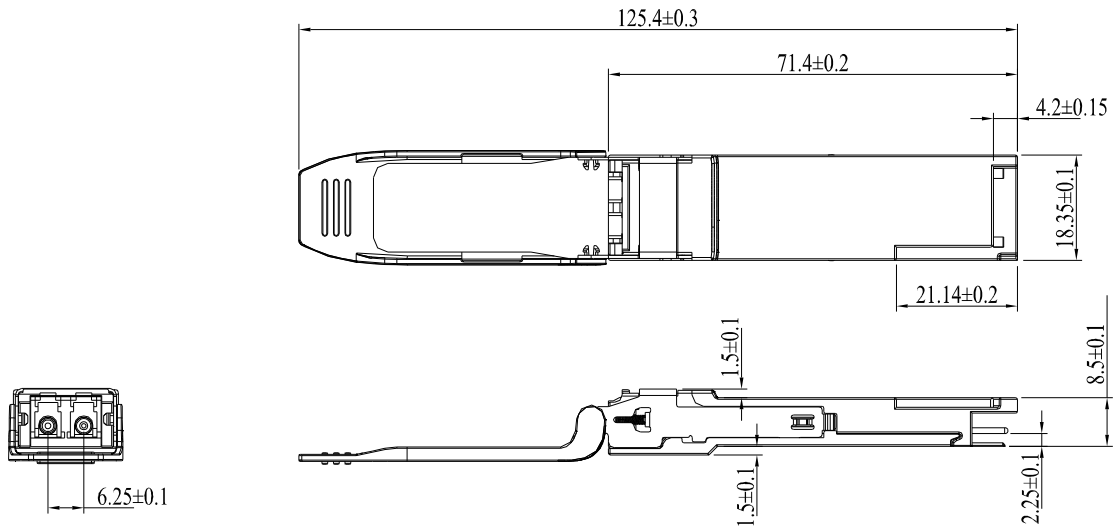
## Host board power supply circuit



## Recommended Interface circuit



## Dimensions



Unit: mm

All Dimensions are  $\pm 0.20$ mm Unless Otherwise Specified





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## Memory Map

