RoHS compliant
TX-1550/RX-1310 nm Single-mode, Single-Fiber (Bi-directional) Transceiver 1×9, SC Simplex Connector, 3.3 V (20dB Margin) 1.25G Gigabit Ethernet

Features

- IEEE 802.3 Gigabit Ethernet
- Industry standard 1×9 footprint
- SC connector
- Single power supply 3.3 V
- Differential inputs and outputs
- Compatible with solder and aqueous wash processes
- Class 1 laser product complies with EN 60825-1

Ordering Information

PART NUMBER	TX	RX	IN/OUT	SD	VOLTAGE	TEMPERATURE	LD TYPE
LSB2-CAL-TC-N5	1550 nm	1310 nm	AC/AC	LVTTL	3.3 V	0 °C to 70 °C	DFB
LSB2-CAL-TI-N5	1550 nm	1310 nm	AC/AC	LVTTL	3.3 V	-40 °C to 85 °C	DFB

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	–40	85	°C	
Supply Voltage	*Vcc*	–0.5	4.0	V	
Input Voltage	V_{IN}	–0.5	*Vcc*	V	
Soldering Temperature	T_{SOLD}	---	260	°C	10 seconds on leads

Operating Environment

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Case Operating Temperature	T_C	0	70	°C	
		-40	85		
Supply Voltage	*Vcc*	3.1	3.5	V	
Supply Current	$I_{TX} + I_{RX}$	---	300	mA	

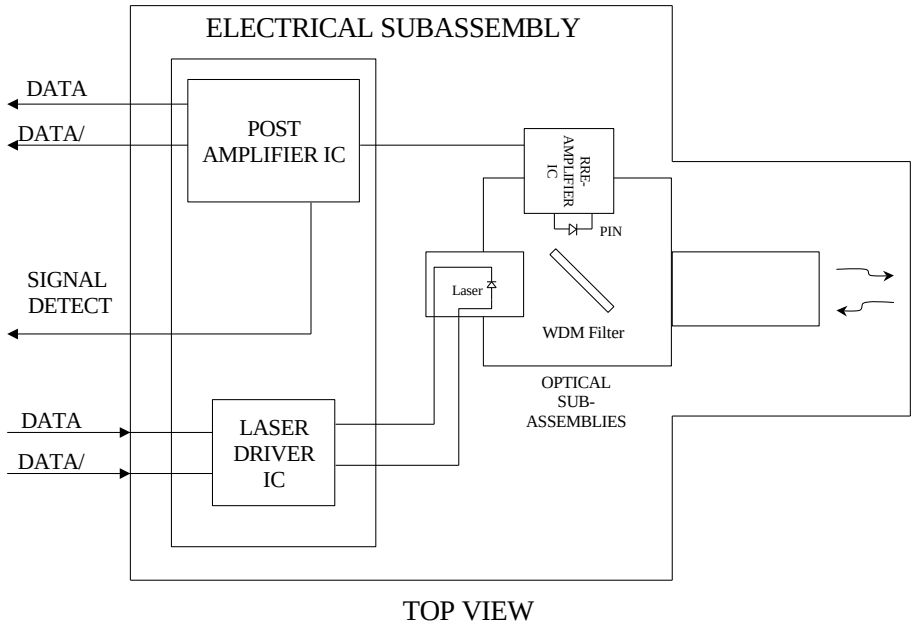
Transmitter Electro-optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate	*B*	---	1250	1300	Mb/s	
Output Optical Power 9/125 μm fiber	*Pout*	–3	---	+2	dBm	Average
Extinction Ratio	*ER*	9	---	---	dB	
Center Wavelength	λ_C	1530	1550	1570	nm	
Spectral Width (-20dB)	$\Delta\lambda$	---	---	1	nm	
Side Mode Suppression Ratio	SMSR	30	---	---	dB	
Rise/Fall Time (20–80%)	$T_{r,\,f}$	---	---	260	ps	
Output Eye			Compliant with IEEE802.3			
Transmitter Data Input Differential Voltage	V_{DIFF}	0.3	---	2.0	V	

Receiver Electro-optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate	B	---	1250	1300	Mb/s	
Optical Input Power-maximum	P_{IN}	0	---	---	dBm	BER < 10^{-12}
Optical Input Power-minimum (Sensitivity)	P_{IN}	---	---	–23	dBm	BER < 10^{-12}
Operating Center Wavelength	λ_C	1260	---	1360	nm	
Return Loss	RL	---	---	–14	dB	λ=1260~1360nm
Signal Detect-Asserted	P_A	---	---	–23	dBm	Average
Signal Detect-Deasserted	P_D	–35	---	---	dBm	Average
Signal Detect-Hysteresis	$P_A - P_D$	0.5	---	---	dB	
Signal Detect Voltage (LVTTL)-High	V_{OH}	V_{CC}–0.8	---	Vcc	V	
Signal Detect Voltage (LVTTL)-Low	V_{OL}	0	---	0.5	V	
Crosstalk	CRT	---	---	–45	dB	
Data Output Rise, Fall Time (20–80%)	$T_{r,f}$	---	---	0.35	ns	
Data Output Differential Voltage	V_{DIFF}	0.6	---	1.2	V	

Block Diagram of Transceiver



Transmitter and Receiver Optical Sub-assembly Section

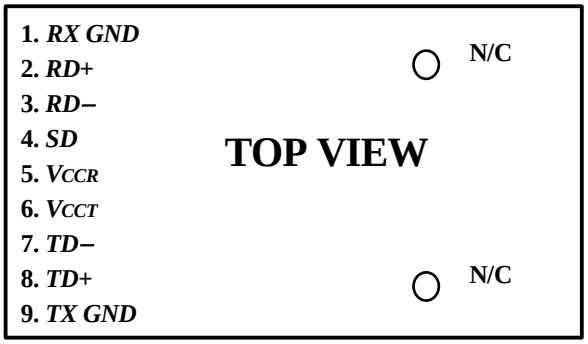
A 1550 nm InGaAsP laser and an InGaAs PIN photodiode integrate with an WDM filter to form a bi-directional single fiber optical subassembly (OSA). The laser of OSA is driven by a LD driver IC which converts differential input LVPECL logic signals into an analog laser driving current. And, The photodiode of OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

Receiver Signal Detect

Signal Detect is a basic fiber failure indicator. This is a single-ended LVTTL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point).

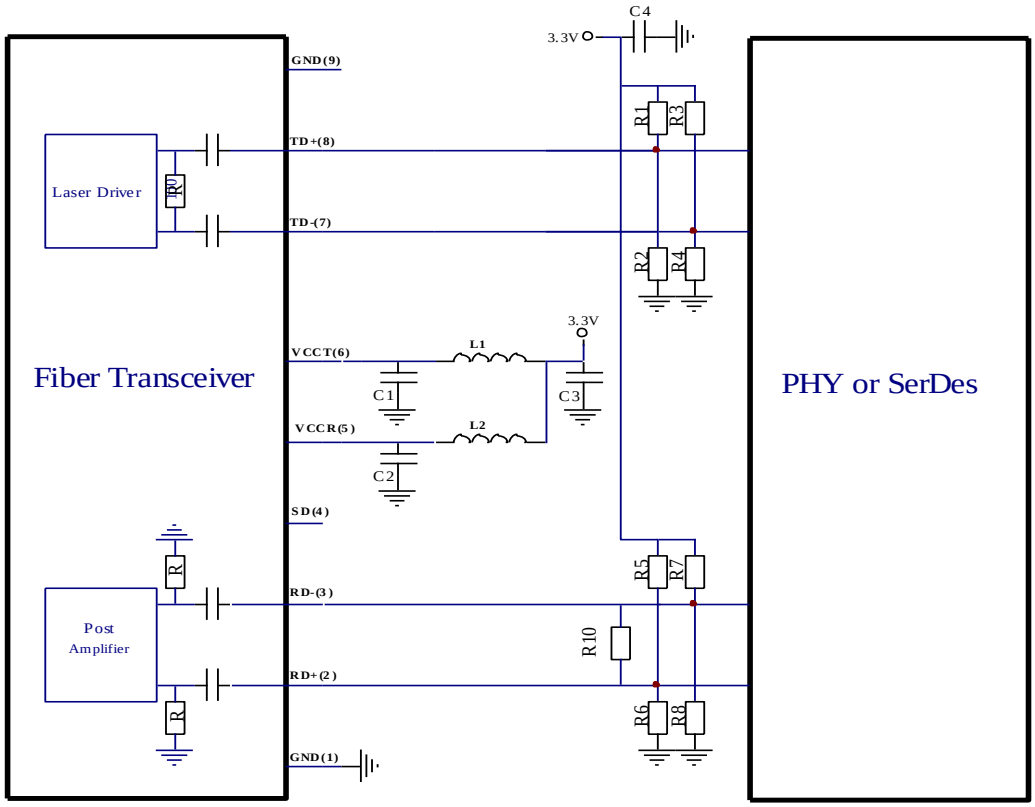
Connection Diagram

Pin-Out



PIN	SYMBOL	DESCRIPTION
1	*RX GND*	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	*RD+*	Receiver Data Output Internally ac coupled. Terminate this differential data output with a 50Ω line and a 50Ω load at the follow-on device (See recommended circuit schematic)
3	*RD–*	Receiver Data Output-Bar Internally ac coupled. Terminate this differential data output with a 50Ω line and a 50Ω load at the follow-on device (See recommended circuit schematic)
4	*SD*	Signal Detect. Normal optical input levels to the receiver result in a logic “1” output, V_{OH}, asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic “0” output V_{OL}, deasserted Signal Detect is a LVTTL output.
5	V_{CCR}	Receiver Power Supply. Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	V_{CCT}	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	*TD–*	Transmitter Data In-Bar. Internally ac coupled. The input stage is internally biased and 50Ω terminated. (See recommended circuit schematic)
8	*TD+*	Transmitter Data In. Internally ac coupled. The input stage is internally biased and 50Ω terminated. (See recommended circuit schematic)
9	*TX GND*	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.

Recommended Circuit Schematic



*C*1/*C*2/*C*4 = 100 nF *C*3 = 4.7 μF *L*1/*L*2 = 1μH

*R*1/*R*2/*R*3/*R*4/*R*5/*R*6/*R*7/*R*8/R10 Depend on SerDes

In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic. When designing the circuit interface, there are a few fundamental guidelines to follow.

(1) The differential data lines should be treated as 50 Ω Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.

(2) For the high speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.

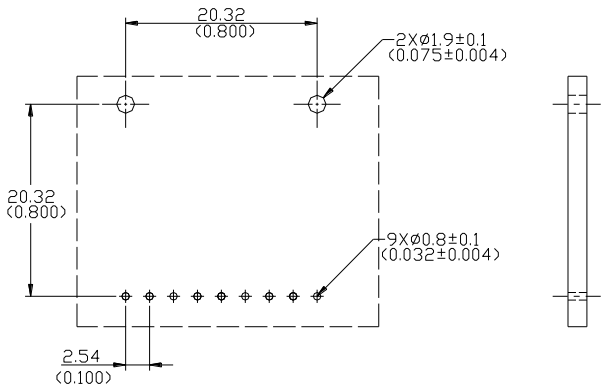
(3) Multi layer plane PCB is best for distribution of V_{CC}, returning ground currents, forming transmission lines and shielding, Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.

(4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress *Vcc* noise over a broad frequency range, this prevents receiver sensitivity degradation due to V_{CC} noise.

(5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1 μF capacitors and a surface-mount coil inductor for 1 μH inductor. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter.

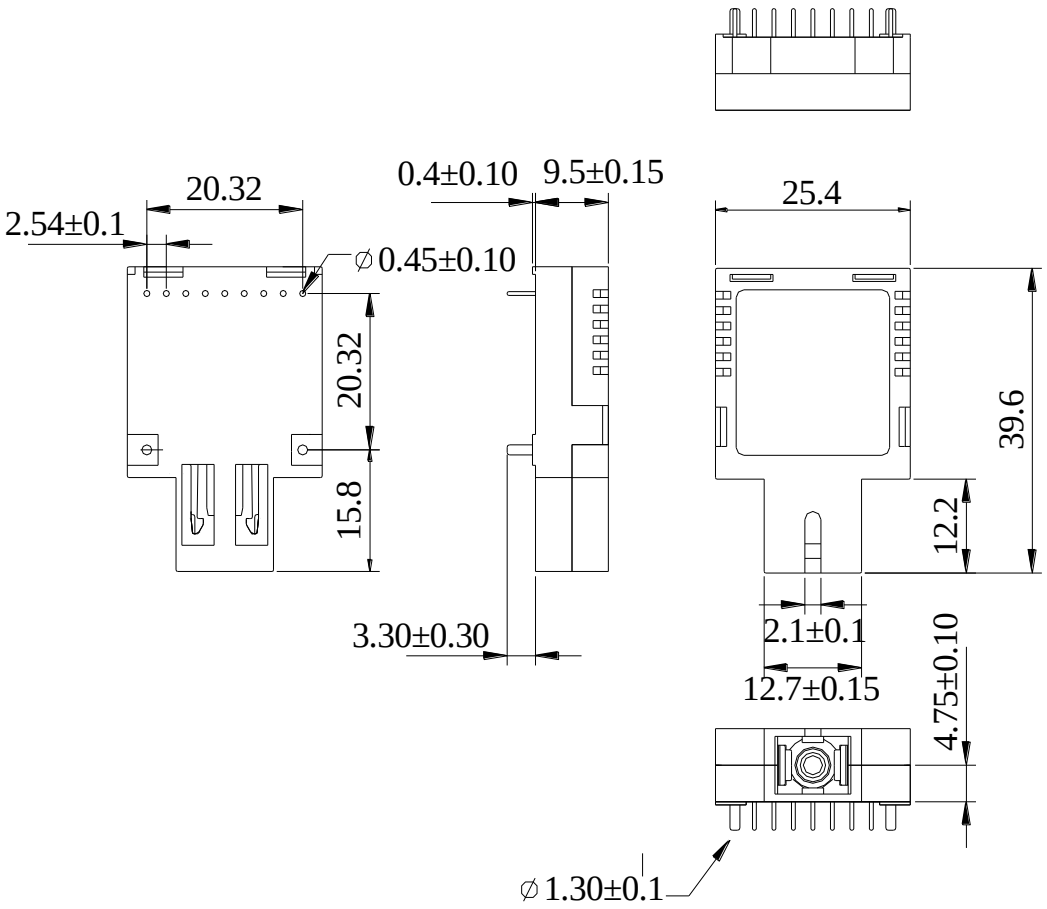
(6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

Recommended Board Layout Hole Pattern



Unit : mm(inches)

Drawing Dimensions



ALL DIMENSIONS ARE±0.20mm UNLESS OTHERWISE SPECIFIED

Unit : mm